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UNIVERSITY OF ALBERTA

BIT-BY-BIT JITTER MEASUREMENT TECHNIQUE

by

©

V.A. ANAND

A THESIS
SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH
IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA
FALL 1990

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Dr. Abu Sesay

Date: 4th June 1990

DEDICATED TO

my father and mother

ABSTRACT

In this thesis, a new bit-by-bit jitter measurement technique is described. This technique has been used to determine the jitter performance of a self-sustaining monostable multivibrator clock recovery circuit.

This jitter measurement scheme provides a time and amplitude quantized histogram estimate for the probability density function of timing jitter. A numerical description of the jitter phenomenon is obtained in terms of the mean and RMS values. It has a measurement precision of the order of 1.7 ps.

An experimental optical fiber transmission system using the NRZ code, with a self-sustaining monostable multivibrator as the timing extraction circuit, was designed and developed. The signalling rate was 50 Mb/s. The signal was transmitted over 5 km of multimode graded index fiber, using a laser diode @ 830 nm and a silicon avalanche photodetector.

The experimental results demonstrate that the measured RMS jitter increases as the number of transitions in the received pattern decreases. It is approximately 2.5° for the "1000 0000 0000 0000" data pattern. The variation of the measured RMS jitter with received optical power indicates that, in the normal operating range, pattern-dependent jitter is the main source of jitter in the recovered clock. The systematic jitter varied between 1.5° to 2° for a 16-bit fixed word pattern, and 2° to 2.5° for PRBS word lengths of $2^{10}-1$ and $2^{23}-1$, respectively. The overall jitter due to fixed or PRBS data patterns and random noise, lies between 3° and 4°, depending on the optical power level.

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LIST OF ABBREVIATIONS

AGC	Automatic gain control
APD	Avalanche photo diode
BER	Bit error rate
BJT	Bipolar junction transistor
BW	Bandwidth
CCITT	Consultative Committee on International Telephony and Telegraphy
DPO	Digital Processing Oscilloscope
DRF	Dielectric Resonator Filter
EX-OR	Exclusive OR gate
FET	Field effect transistor
FWHM	Full width at half maximum
IC	Integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
ISI	Intersymbol interference
LPF	Low pass filter
M-PSK	M-ary phase shift keying
MECL	Motorola emitter coupled logic
MM	Monostable multivibrator
NRZ	Nonreturn-to-zero
PAM	Pulse amplitude modulation
PDF	Probability density function
PLL	Phase-locked loop
PRBS	Pseudo-random binary sequence
PWM	Pulse width modulation

RF	Radio frequency
RMS	Root mean square
RZ	Return-to-zero
SAW	Surface-acoustic wave
SNR	Signal-to-noise ratio
UI	Unit interval

CHAPTER 1

INTRODUCTION

Digital transmission has become reasonably well established as the basis for modern telecommunication networks all around the world. Its primary advantage, compared to analog transmission, is that it offers an inherent noise immunity which can provide an end-to-end transmission quality almost independent of distance; secondary advantages include increased capacity on existing networks, compatibility with digital switching, and simple interfacing with the growing proportion of data traffic from digital sources. The feasibility of such networks is dependent on the attainment of substantially impairment-free operation, irrespective of the traffic carried, with transmission links connected directly together in tandem, or indirectly through digital switches and multiplex equipment [1].

Although the noise immunity of digital systems is high, relatively sharp thresholds exist which, if exceeded, result in a rapid deterioration of system performance. Amplitude noise in digital systems can be controlled by regeneration. Timing noise, usually known as "**timing jitter**", displaces the transitions between adjacent digits, and is not so easily controlled, because of the practical and economic difficulties of obtaining jitter-free clocks for regeneration at points remote from the original clock source. Timing jitter is especially important because the information content of digital signals is essentially carried by the transitions between digits and a knowledge of the expected digit spacings; timing jitter affects both of these and, like noise, has cumulative properties so that, without adequate control, it can grow to an amplitude such that the jittered clock will sample the data at non-ideal times.

A digital telecommunication system must operate correctly in the presence of jitter and hence the topics of jitter origination, accumulation, and control, are important in any digital system. It is the objective of this project to measure the jitter variance in an optical fiber communication system, to determine its statistical properties and to study how jitter degrades the bit error performance.

1.1 Definition of Jitter

In an ideal digital transmission system, the pulses of the digital pulse stream would arrive at times that are integral multiples of the pulse repetition period T. However, in real systems, pulses arrive at times that differ from the ideal times of integral multiples of T. This unwanted pulse position modulation of the pulse stream is called "**Jitter**". Jitter is formally defined by the CCITT as short-term variations of the significant instants of a digital signal from their ideal positions in time. Longer-term variations are defined by the CCITT as "**wander**". The "significant instant" referred to in the definition can be any fixed arbitrary point on a digital signal that is clearly identifiable, such as the leading or trailing edges, or the mid-points of pulses. Figure 1.1a shows a train of unit impulses initially spaced equally in time; after either transmission or signal processing these unit impulses become spaced slightly irregularly in time (Figure 1.1b). The time deviations from integral multiples of T form a discrete time, continuous amplitude sequence e[nT]. This sequence represents the fundamental description of jitter; e[nT] has dimensions of time in amplitude, at integer multiples of T. Throughout this thesis, square brackets denote a discrete time function, while

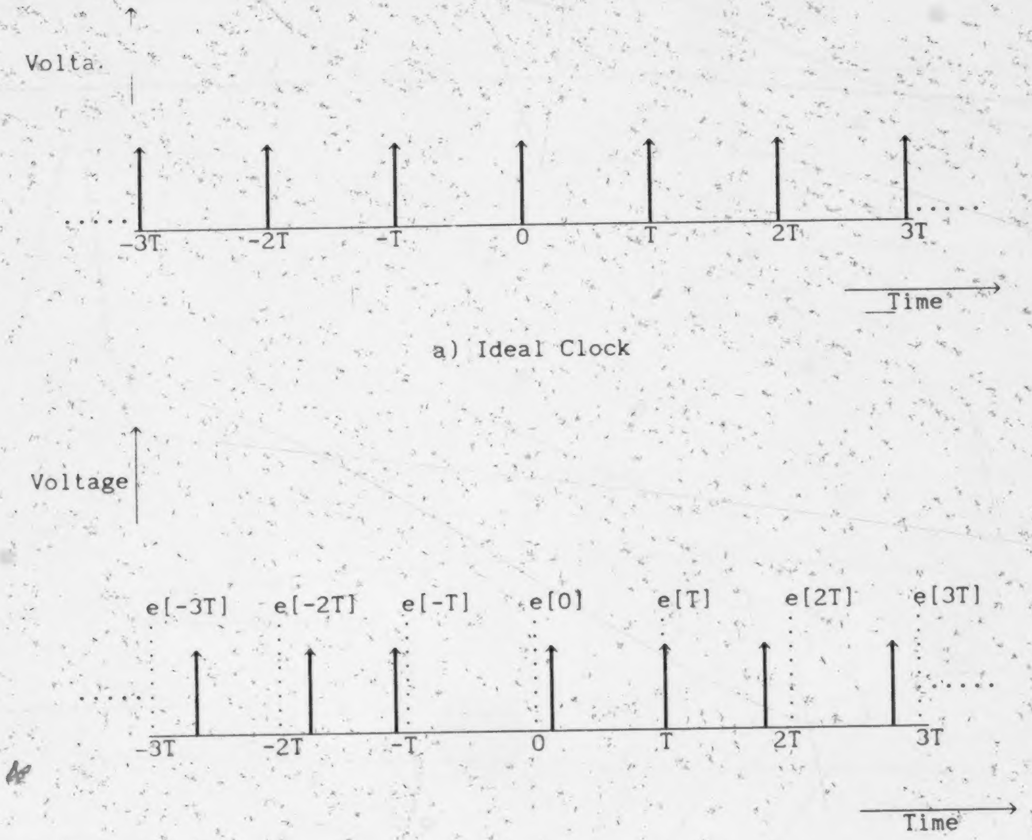

Volta
-3T
-2T
-T
0
T
2T
3T
Time
a) Ideal Clock
Voltage
e[-3T]
e[-2T]
e[-T]
e[0]
e[T]
e[2T]
e[3T]
-3T
-2T
-T
0
T
2T
3T
Time
b) Jittered Clock

Fig. 1.1 Defining Jitter. Jitter is the effect of the real clock edges varying in time relative to ~~an~~ ideal clock [2].

parentheses denote a continuous time function. The units in which jitter amplitudes are specified and measured are generally in terms of the unit interval (UI), which is equal to one bit period, or in terms of phase, by defining one bit period T as equal to 360°. In digital transmission systems e[nT] is a random function of time called a stochastic process [2].

1.2 The Importance of Timing in Digital Systems

Digital telecommunication systems invariably use serial digit transmission, and the ability to be able to correctly identify each digit at any point in a system is of the utmost importance. The inherent noise immunity of digital signals allows substantially error-free decisions to be made on the magnitudes of individual digits in the presence of significant noise, but this is only possible if the digits are correctly identified in time from the preceding or succeeding digits. When an optical signal is transmitted along an optical fiber, dispersion mechanisms within the fiber cause broadening of the optical pulses as they travel along the channel. This causes distortion in both digital and analog transmission. The amount of broadening depends on the distance that the optical pulses travel along the optical fiber before they are regenerated. The dispersion or broadening of the pulses may occur to such an extent that neighbouring pulses may start to overlap one another, and thus become indistinguishable at the receiver input. This effect is known as *Intersymbol Interference (ISI)*.

In the presence of ISI, the digital symbols have rise and fall times of the order of a symbol period. For no overlapping of light pulses to occur in an optical fiber link, the maximum bit rate B_T or transmission bandwidth (for return-to-zero pulses) should be less than the reciprocal of the broadened pulse duration (2τ), i.e.

$$B_T \le 1/2\tau.$$

ISI may be reduced by equalization, where a filter is used to partially restore the shape of the pulses. Figure 1.2 shows an eye diagram which is open, and where the decision time corresponds to the centre of the eye opening. The effect of ISI and noise is to close the eye pattern. In this case the margin against amplitude noise (or in other words, the SNR), decreases rapidly as the decision time moves away from the nominal centre of the eye. Thus, the presence of timing jitter will cause an average decrease of SNR, and a consequent increase in the BER.

1.3 Clock Transmission and Recovery

In baseband digital systems, the output of the receiver must be sampled at precise sampling instants in order to recover the original signal. To perform this sampling, a clock signal is needed at the receiver that is synchronized with the clock signal at the transmitter. Three general methods by which this synchronization can be obtained are [71]:

a) derivation of clock information from a primary or secondary standard; for example, the transmitter and receiver can be slaved to a master clock through a separate channel.

b) transmitting a synchronizing clock signal over the same channel as the signal.

c) derivation of the clock signal from the received signal waveform itself.

The first method is often employed in large data communication networks. Due to the high cost of this method, point-to-point data

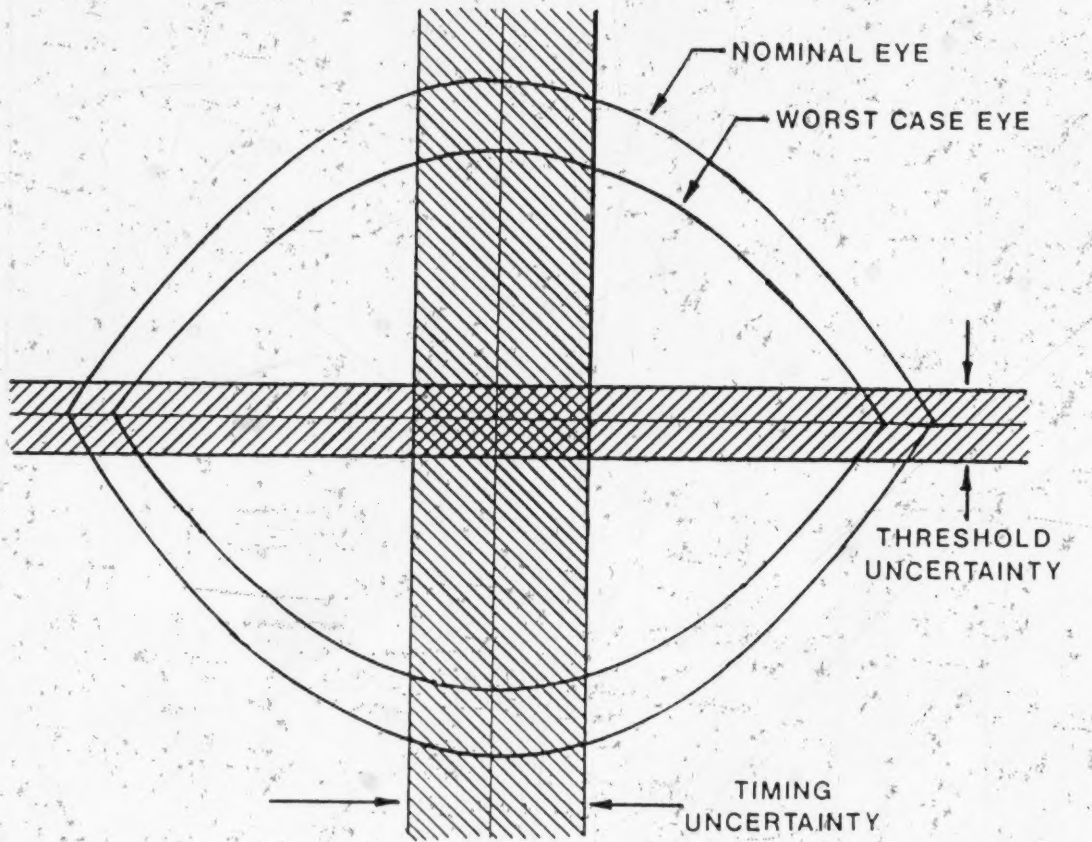

NOMINAL EYE
WORST CASE EYE
THRESHOLD UNCERTAINTY
TIMING UNCERTAINTY

FIG.1.2 EYE PATTERN IMPERFECTIONS FOR CLOCK RECOVERY

transmission normally does not use this method. A more economical method is to transmit the clock signal along with the data, which means that a small part of the channel's information capacity is used by the clock signal. The third method, known as *self-synchronized* or *self-timed*, is a very efficient method of synchronization between receiver and transmitter. Digital transmission equipment is generally arranged to be self-timed, with timing signals or clocks derived by nonlinear processing of the incoming digital signal. This process is known as timing extraction [3]. This processing yields two frequency-domain components. The first, consisting of discrete spectral lines at the symbol rate and its harmonics, results from the periodic nature of the symbols; the other component, which is continuous and somewhat noise-like, arises from the information content or line coding of the digital signals. The timing clock may be recovered from the symbol rate component by the use of a narrowband bandpass filter, which usually consists of a simple LC "tank" circuit, a surface-acoustic-wave (SAW) device, or a phase-locked loop (PLL).

Practical bandpass filters, having nonzero bandwidths, will pass not only the required spectral line components but also that part of the continuous spectrum adjacent to the spectral line. These unwanted sidebands effectively modulate the recovered clock both in amplitude and phase, the latter appearing directly as *timing jitter*. A useful figure of merit is the ratio between the power contained in the discrete clock spectral line to the power contained in the continuous spectrum that falls within the passband of the clock recovery circuit. In practice, amplitude modulation may also cause additional jitter through the process of amplitude-to-phase conversion. The suppression of this amplitude and phase modulation is determined by the timing recovery filter bandwidths, and is limited by the tuning accuracy and stability of the filters. Mistuning of a filter passband centre frequency relative to the symbol rate gives rise to pattern-sensitive timing jitter in the recovered clock, which can result in large phase transients [4]. The amplitude of the recovered clock is proportional to the timing density or number of transitions per unit time between symbols in the transmission code, and amplitude variations can therefore be limited by the use of a line code having suitable bounds on its timing density. (Line coding in fiber optics is discussed in the next section).

Intersymbol interference resulting from bandwidth restrictions and misequalization in the transmission path also causes jitter through pulse shape variations, and hence spectral variations, at the timing recovery filter input.

Any jitter present on a recovered clock will be imparted to the digital data stream in any associated processing such as regeneration. Jitter within the timing recovery bandwidths of a digital transmission system is therefore added to the regenerated signals in a cumulative manner. Unfortunately, the predominant sources of jitter tend to be additive since they are related to modulation components of the digital signals; the accumulation of this jitter is consequently more rapid than that of jitter from noncoherent sources. This is one of the factors which could, if not properly controlled, limit the performance of a digital network.

1.4 Line Coding in Optical Fiber Communications

The function of coding is to adapt a signal source to a transmission medium for the purpose of efficient and reliable communications. The subject of coding is divided into source coding and channel coding [5]. *Source coding* is the conversion of the messages produced by a source into a string of binary digits. *Channel coding*, on the other hand, is the transformation of the binary digits generated by the source into a form suitable for a specific transmission medium. *Line coding* is a subset of channel coding that normally does not include error correction codes and is mainly concerned with matching the transmitted signal spectrum to the transmission characteristics of the channel, so as to limit impairments such as timing jitter, ISI, baseline wander, etc. [6].

A line code that is attractive for optical fiber communications should possess the following characteristics [7-11]:

a. Frequent transitions.
b. Zero dc and small low frequency content.
c. Two level (binary).
d. Bit sequence independent.
e. Bandwidth efficient.
f. Moderate redundancy.
g. Simple implementation.

A brief discussion of the desirability of some of these requirements is now presented. The line code must have frequent transitions in order that a stable clock signal (with minimum jitter) may be extracted at the receiver, as explained in the earlier section. Furthermore, the longest interval between transitions must be restricted to a small value in order to prevent the clock recovery circuit from falling out of lock with the data source and losing synchronization. Ideally, the line code should provide a transition for every source bit.

The dc component in the signal power density spectrum should be zero and the low frequency components should be small, in order to minimize baseline wander, which is the shifting of the receiver output in the presence of a long string of ones or zeros due to AC coupling in the receiver. Baseline wander is undesirable because it results in a reduction of the signal amplitude at the sampling instant, and hence in a reduced receiver sensitivity.

The optical signal should be binary, due to the unipolar nature of light intensity. Multilevel transmission increases the information capacity of a fiber optic channel, but suffers from the following problems:

a) Due to signal-dependent shot noise, the receiver threshold levels for multilevel systems need to be non-uniformly spaced, which complicates the receiver design.

b) Lasers are non-linear devices, making the generation of multilevel signals more difficult than the generation of binary signals.

A line code is bit sequence independent if the communication link can function properly regardless of what bit stream is emitted by the source. For example, if the message source were to emit all ones, the line code should still provide sufficient transitions so that the system performance would not degrade due to baseline wander or drifting of the clock signal. In general, a line code is bit sequence independent if it contains only a small amount of low frequency energy; i.e., a long string of ones or zeros is not possible.

In high bit rate systems, a careful choice of line code with as little redundancy as possible is required especially when the pulse dispersion is significant [12]. The required system bandwidth is proportional to the amount of redundancy added. As the system bandwidth increases, the noise power at the receiver output increases, and the receiver sensitivity decreases. Several line codes for fiber optic communications have been proposed previously. These include simple 1B2B codes (where one data bit is coded by two line code pulses, see Figure 1.3) such as the Manchester Code [13], Miller Code [8], or Petrovic Code [14] and some other complex block codes such as the 3B-4B, 5B-6B, 7B-8B and 13B-14B codes [12-22]. However, the majority of commercial fiber optic systems developed to date employ the nonreturn-to-zero (NRZ) format because of its simplicity of implementation. The NRZ code finds wide application in long haul systems where it is necessary to minimize the system bandwidth and maximize the receiver sensitivity. Among the two-level codes, the NRZ code requires the least amount of bandwidth and provides the greatest sensitivity for a given data rate. A data scrambler is required because the NRZ code can give rise to a long string of ones or zeros, which may cause base line wander problems at the receiver. As mentioned earlier, this is due to the nonzero power spectral density at dc ($\omega = 0$), of the NRZ code. Also, the NRZ code has the disadvantage that it has no error detection or correction capability. Figure 1.4 shows the power spectral density of various binary line codes [14].

The NRZ type of line coding was used in this thesis, without a data scrambler. The main reason for using this code is as follows:-

a) Simple to use, as it requires no coder or decoder.

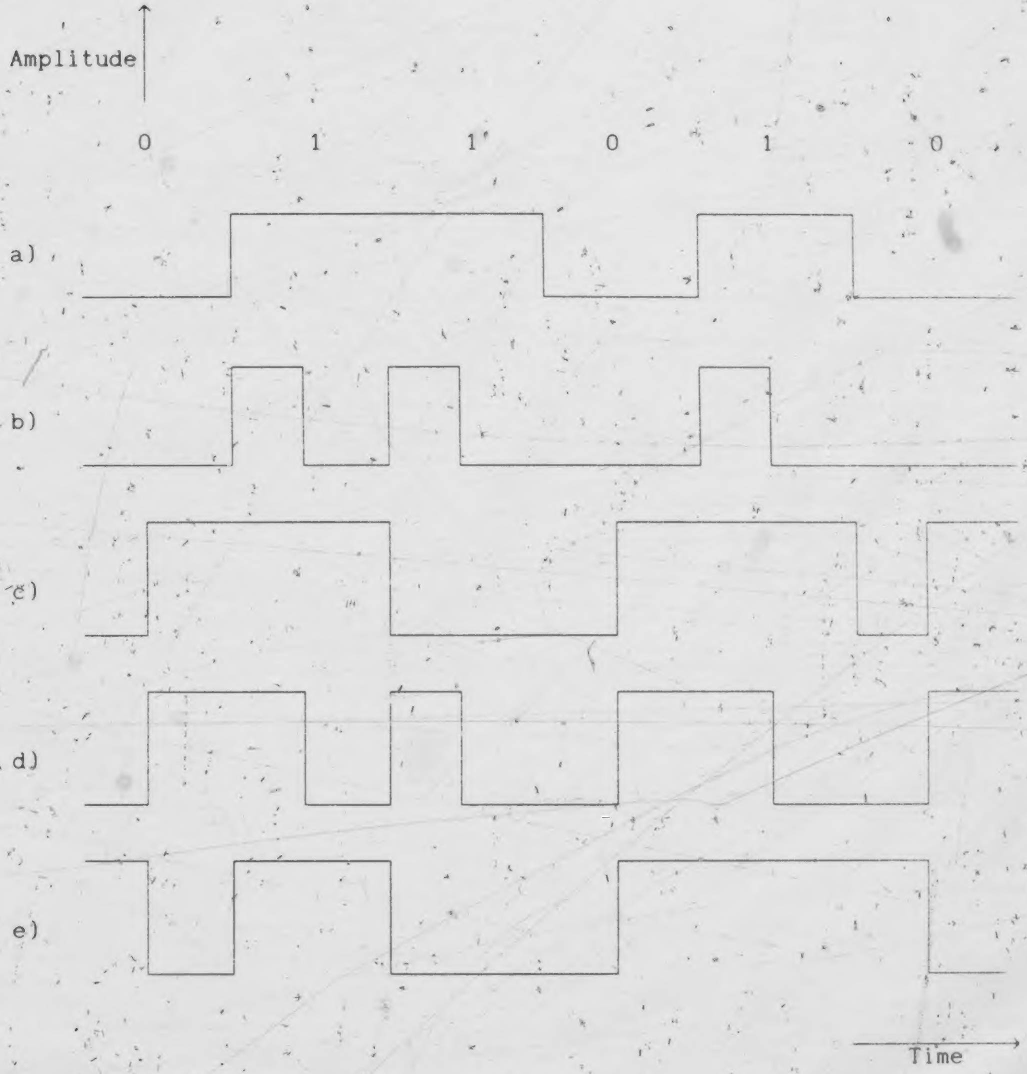

Amplitude
0
1
1
0
1
0
a)
b)
c)
d)
e)
Time

Fig. 1.3 Different Binary Line Codes

a) NRZ
b) RZ
c) CMI
d) Manchester
e) Petrovic

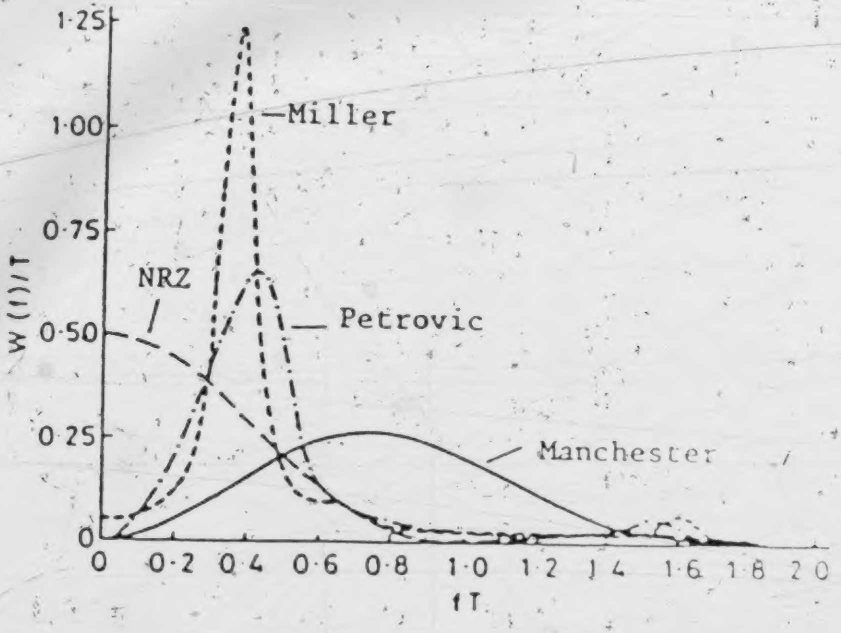


Fig. 1.4 Power Spectral Density of Various Binary Line Codes [14].

b) Most of the commercial fiber optic systems use the NRZ code.

c) It is interesting to study the timing jitter behaviour of the NRZ code without a data scrambler, since, in this case long sequence of ones or zeros may be present. Thus, the timing jitter should be worse than any of the other binary level codes, which have control over the number of continuous ones or zeros that may occur. Hence, it is worthwhile to study the timing jitter behaviour of the NRZ code, since all other line codes would give better results no matter which method of clock recovery is employed.

1.5 An Optical Fiber Communication System

Figure 1.5 shows the block diagram of a basic digital fiber-optic communication system. **M** electrical data signals, with well defined and standardized rate, line code, and pulse shape, arrive at the multiplexing terminal. These **M** electrical signals are synchronized, the necessary overhead bits are added, and the signals are then interleaved to form a higher rate electrical signal [2]. The electrical multiplexer output signal is clocked by a local timing signal. Therefore, the output pulse stream leaves the multiplexer with negligible jitter with respect to the local multiplexer output clock. However, the primary sources of jitter in digital transmission systems are regenerators and multiplexers. The process of synchronizing and inserting overhead bits onto the tributary signals results in jitter appearing on the tributaries after demultiplexing. In this thesis, we concentrate only on the jitter introduced by the line regenerators.

The high speed electrical signal which is now the source of binary ones and zeros is coded by the encoder. There are many code formats by which the binary data may be coded, the most common being the

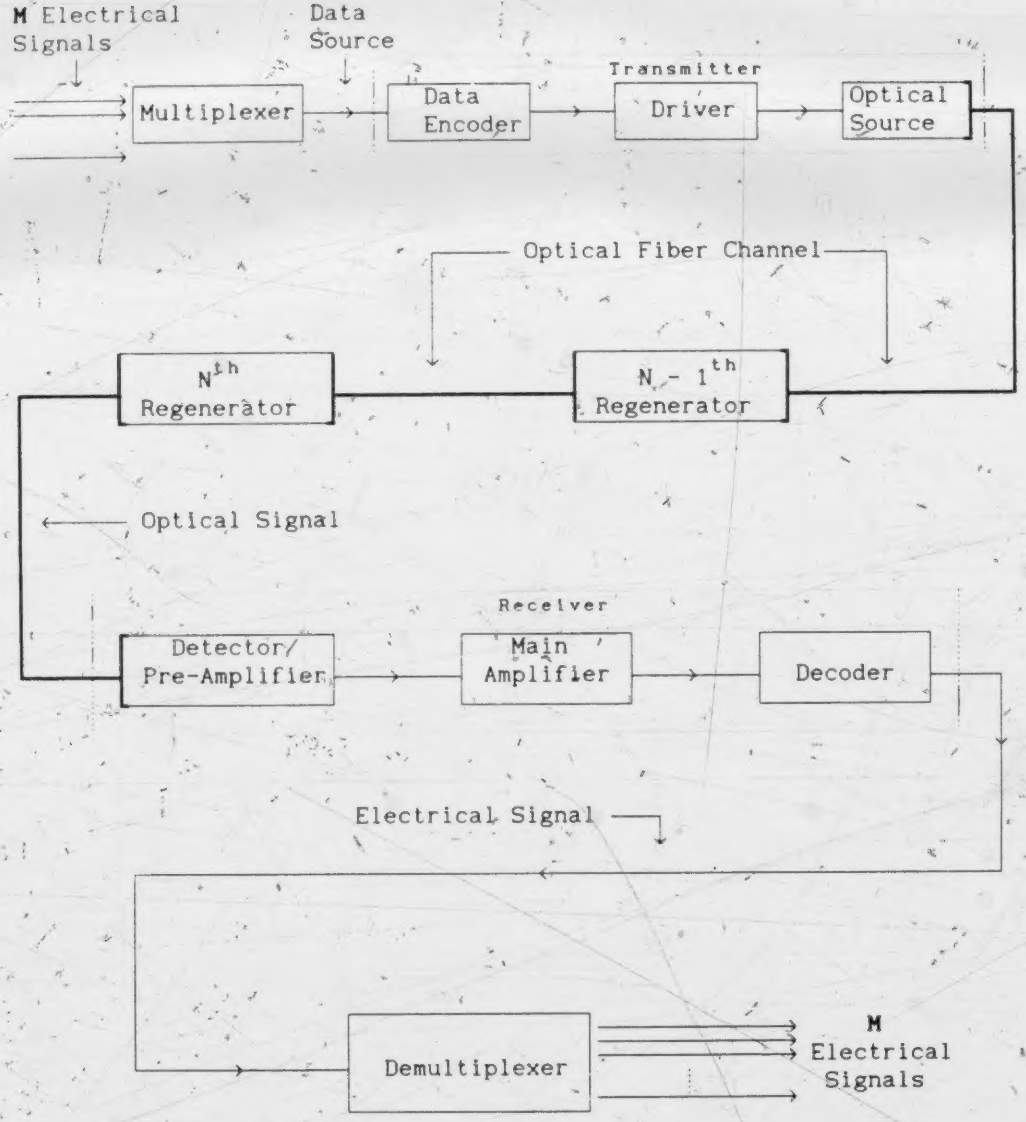

M Electrical Signals
Data Source
Transmitter
Multiplexer
Data Encoder
Driver
Optical Source
Optical Fiber Channel
N^{th} Regenerator
$N - 1^{th}$ Regenerator
Optical Signal
Receiver
Detector/ Pre-Amplifier
Main Amplifier
Decoder
Electrical Signal
Demultiplexer
M Electrical Signals

Fig. 1.5 Block Diagram of a Digital Optical Fiber Communication System.

nonreturn-to-zero (NRZ *coding*) which is examined here. The coded electrical data then drives a laser transmitter that generates a light signal whose intensity is proportional to the signal-dependent injection current. The requirements of an optical source for a high bit rate link are a narrow spectral width, a small beam area, a high electrical-to-optical power conversion efficiency, good high frequency response, a long life span and the emission of light at wavelengths that are compatible with the optical fiber characteristics. The transmission channel could be single-mode or multimode fiber, depending on the system requirements.

After transmission through the fiber, the optical signal is converted back to an electrical signal using either a PIN or *avalanche photodiode* (APD). The signal after detection is corrupted by two sources of noise. These are (a) the photodiode shot noise and (b) the receiver thermal noise. In the case of fiber optic systems using direct detection and PIN photodiodes or APDs with average gains less than twenty, shot noise can be neglected [2]. Also, in most cases, it is the thermal noise of the preamplifier which dominates the total noise of the receiver. Hence, we assume that the overall noise is mainly due to the receiver thermal noise and that shot noise is negligible. For this condition the noise will have Gaussian statistics. Once the electrical signal is amplified and reshaped, a timing signal will be extracted from it and the regenerated electrical data signal will be produced. This regenerated signal can either go to another laser transmitter in the case of a regenerator (a back-to-back receiver-transmitter combination), or, at the end of the system to a demultiplexing terminal. At the demultiplexing terminal the higher rate electrical signal is separated into its tributaries, the overhead bits are removed, and the **M** electrical signals are recovered.

1.5.1 Fiber Optic Regenerator

Digital transmission systems, in particular fiber-optic transmission systems, use line regenerators to send information over longer distances than is possible through a single laser-fiber-receiver span. The line regenerator receives the weak and dispersed incoming optical signal, and attempts to regenerate the original signal as closely as possible, for retransmission by its laser transmitter. When regenerators are cascaded an accumulation of jitter results [2].

Figure 1.6 shows the block diagram of a self-timed fiber optic regenerator. An optical receiver containing a photo-detector converts the optical signal from the incoming optical fiber into an electrical signal. As the output signal from this detector is normally very small, a low noise preamplifier is used, coupled directly to the photo-detector to amplify the signal level with minimum noise penalty. A certain amount of thermal noise is introduced by this preamplifier, and an APD is often preferred to a PIN photodiode, in order to achieve a higher receiver sensitivity [23]. For a transmission channel degraded by white noise, the noise level increases linearly with increasing channel bandwidth. Hence a filter is normally incorporated into the receiver to limit the noise. The optimum bandwidth of the filter depends on the signal bandwidth, and is chosen to maximize the signal-to-noise ratio (SNR).

The main amplifier further amplifies the signal to a voltage level that can trigger the clock recovery and decision circuits. This amplified electrical signal is then passed through an equalizer and an

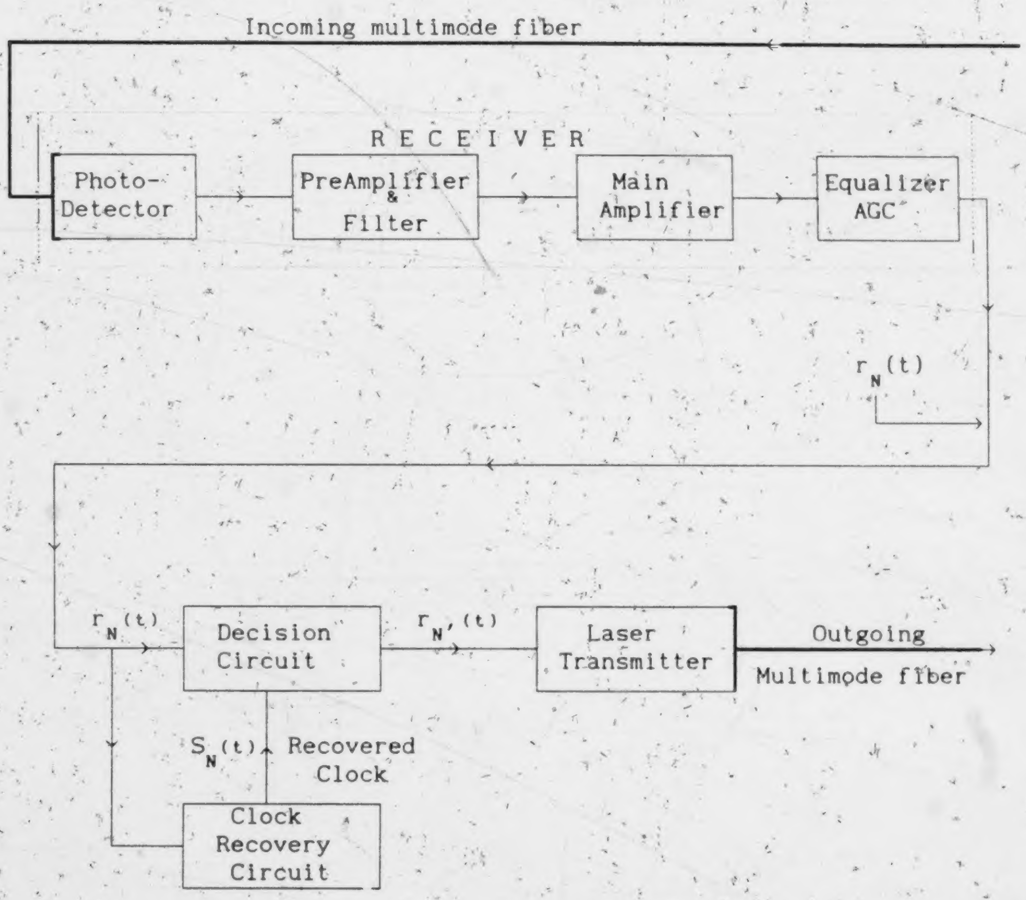

Incoming multimode fiber
RECEIVER
Photo-Detector
PreAmplifier & Filter
Main Amplifier
Equalizer AGC
$r_N(t)$
$r_N(t)$
Decision Circuit
$r_N'(t)$
Laser Transmitter
Outgoing
Multimode fiber
$S_N(t)$
Recovered Clock
Clock Recovery Circuit

Fig. 1.6 Block Diagram of a Self-timed Fiber Optic Regenerator

automatic gain control (AGC) amplifier that produces an output signal $r_N(t)$. The function of the equalizer is to reduce intersymbol interference (ISI). The signal $r_N(t)$, received by the Nth regenerator in a long chain of cascaded regenerators, is corrupted by receiver noise and jitter accumulated from the previous N-1 regenerators. We express $r_N(t)$ as

$$r_N(t) = \sum_{n=-\infty}^{+\infty} a_n \, g_N(t-nT-e_{N-1}[nT]) + \eta_N(t) \qquad \ldots\ldots(1.1)$$

where $a_n \in \{0, 1\}$, $g_N(t)$ is the amplified and equalized received pulse, $\eta_N(t)$ is additive receiver noise, and $e_{N-1}[nT]$ is the time deviation from time nT of the Nth pulse's zero crossing. The $e_{N-1}[nT]$ jitter sequence is the accumulated jitter from the previous N-1 regenerators.

The received signal is sampled by the decision circuit and a regenerated output signal is produced, based on decisions made about $r_N(t)$ at the sampling instants. The timing signal used for sampling is derived from the timing extraction circuit, which extracts either a sinusoidal waveform or a square wave of frequency 1/T from $r_N(t)$. Since timing extraction is imperfect, the timing signal is given by

$$s_N(t) = |A_N| \sin\left[\frac{2\pi}{T}(t-e_N(t))\right] \qquad \ldots\ldots(1.2)$$

where $|A_N|$ is a constant amplitude, and $e_N(t)$ is the jitter on the timing signal, which is a continuous time phase modulation of $s_N(t)$; $e_N(t)$ is caused by imperfections of the timing extraction process, the input jitter $e_{N-1}[nT]$, and the receiver noise $\eta_N(t)$.

When $s_N(t)$ rises to a voltage V, $r_N(t)$ is sampled and the decision circuit creates a regenerated output signal, that in turn modulates a laser transmitter. The regenerated output signal is given by

$$r'_N(t) = \sum_{n=-\infty}^{+\infty} a'_n \, f_N(t-nT-e_N[nT] + \tau + t_o) \qquad \ldots\ldots(1.3)$$

where a'_n is the regenerated bit sequence, $f_N(t)$ is the output pulse, t_o and τ are static phase shifts and $e_N[nT]$ is the output jitter of the Nth regenerator, a sampled $e_N(t)$. The term t_o is caused by the non-zero sampling threshold of the decision circuit. A $V = 0$ sampling threshold eliminates this static phase shift. Hence, DC offsets in the sampling portion of the decision circuit should be minimized. The static phase offset τ is caused by the physical separation of the timing and decision circuits. This static phase alignment between the data and the timing signals must be set either by choosing the length of a coaxial cable between the timing and decision circuits or by some electronic phase shifting network so that the data signal is sampled at an optimum time. Therefore, the timing signal jitter is impressed onto the output data signal. Equations (1.1) to (1.3) mathematically describe the signal processing carried out in a line regenerator. We see that jitter is present on both the input and the output signals.

Without adequate control, it is possible for timing jitter to accumulate in digital networks to the extent that it could degrade the overall performance. This could happen in two ways.

a) Jitter can increase the probability of error, by causing the signal sampling time instants to deviate about the eye centre and thus lead to a reduction in the SNR.

b) In the case of a digitally encoded analog signal, jitter in the bit stream arriving at the decoder finally leads to the decoded analog samples appearing in a slightly irregular manner. This is sometimes known as "**absolute jitter**" [1,27,30,31].

Digital impairments such as errors are dependent on the difference between the jitter on the received signal to be sampled and the jitter on the extracted clock signal that determines the sampling times. This relative difference is known as "**alignment jitter**" [29,32].

1.6 Thesis Objectives and Organization

1.6.1 Objectives

The purpose of the research work reported in this thesis is to study the jitter performance of an all-digital, self-sustaining monostable multivibrator clock recovery circuit in a fiber optic communication system. Having done this, it was proposed to study experimentally, the performance of a fiber optic transmission system in terms of the bit error rate (BER) in the presence of timing jitter. To keep the project scope within the M.Sc. range, the investigation was limited to the study of only the jitter performance of the monostable clock recovery circuit.

Hence, the main objectives of this thesis are as follows:

1. To develop a bit-by-bit jitter measurement technique to determine the statistics of the jitter phenomenon.

2. To develop a computer program to control the digitizing oscilloscope in order to make the acquisition to and transfer the data on to the computer.

3. To develop a computer program to process the data and determine the mean, variance and probability density function (pdf) of the timing jitter.

4. To design and develop a monostable clock recovery circuit. An experimental optical fiber transmission system operating at 50 Mb/s was then set up.

5. To experimentally measure the RMS jitter as a function of various data patterns, and to study the time dependent nature of the jitter probability density function.

6. To experimentally measure the RMS jitter against received optical power for various data patterns, so as to obtain the relationship between the systematic and random components of the jitter and the signal-to-noise ratio.

1.6.2 Organization

Chapter 1 introduces the topic of jitter, clock recovery and the importance of timing in digital systems. We also present the characteristics that a line code should possess in optical fiber systems, how the NRZ code compares to these characteristics and why we chose to work with this code.

Chapter 2 deals with the theoretical analysis of timing extraction and jitter in self-timed regenerators. It presents the various sources of jitter, a theoretical justification of the existence of a timing signal at the signalling rate and the process of clock extraction. It also introduces the topics of accumulation of jitter in long haul fiber-optic systems with several repeaters, and the performance of an optical communication system in the presence of jitter.

Chapter 3 describes the self-sustaining monostable clock recovery circuit and analyze its clock jitter. A simple modification to the original clock recovery circuit will be proposed. Chapter 4 reviews the various jitter measurement techniques, the method that was tried at first,and the method finally used. The experimental fiber-optic system and the jitter measurement system will be described in chapter 5.

Chapter 6 will present the experimental results that were obtained. It will show that the clock jitter increases as the number of transitions in the received bit sequence decreases. In the normal operating range of the receiver, it is found that the effect of random noise on the jitter is quite small, and that pattern-dependent jitter is dominant. The random jitter is dominant only at very low optical power levels. Chapter 7 presents a summary of the results, together with the conclusions. Suggestions for further research in this area are also given.

CHAPTER 2

TIMING EXTRACTION AND JITTER

this chapter the various sources of jitter are discussed. The structure of the received signal will be explored to show that it contains timing information which can be used to reconstruct the clock signal. A mathematical analysis of a clock recovery circuit using an Exclusive-OR gate as a non-linear element is presented to show that it generates a discrete spectral line at the symbol frequency. Finally, the accumulation of jitter in a long haul system with several repeaters and the effect of jitter on the performance of a communication system are presented.

2.1 Sources of Jitter

Jitter can arise from a variety of sources in digital transmission systems and networks. The majority of sources fall into one of the following categories [24].

2.1.1 Jitter produced by the Electronic Components

Two mechanisms account for the presence of jitter on timing signals originating from oscillators. The first is the intrinsic phase noise generated by components, called *flicker noise*, and the second is the *phase noise* in logic circuits arising as a result of signal transition uncertainties. Both of these are dominated by low frequency components. This jitter is usually negligible compared to other mechanisms.

2.1.2 Jitter produced by the Digital Regenerators

2.1.2.1 Systematic (pattern-induced) Jitter

Most of the significant sources of jitter produced by digital regenerators are strongly dependent on the pattern content of the digital signal being transmitted [25-29]. The continually changing patterns of the digital signals produce spectral components which fall within the passband of the timing recovery filter, and hence cause variations in the time of occurrence of the recovered clock. These effects are augmented by other repeater imperfections such as intersymbol interference, pulsewidth effects and amplitude-to-phase conversion as described earlier. Values for systematic jitter for a single regenerator typically fall in the range of 0.4 to 1.5% of a unit interval r.m.s., for all data rates [30].

2.1.2.2 Random Jitter

Random sources of jitter in regenerative repeaters include differential pulse delay in the output stages of repeaters for multilevel transmission codes, non-systematic mistuning of the timing recovery filter resulting from incorrect initial adjustment and aging, temperature and other environmental effects, noise, interference and crosstalk.

2.1.3 Jitter produced by the Optical Systems

Optical transmission systems produce an additional timing jitter contribution from sources such as laser control circuits, optical receiver noise, mode hopping, and dispersion [1].

2.1.4 Wander

Variations in the propagation delays of cables resulting from temperature changes can cause an apparent phase change of several tens of bit periods over a long period of time. Such variations occur very slowly and are considered as *wander*.

2.2 Existence of Timing Signal

For complete regeneration, a local source of timing information is required at each regenerator. The preferred means of providing this is by extraction of the timing information from the received signal. By performing a spectral analysis of the received signal we can show that it contains a discrete component at the pulse repetition frequency. The spectral characteristics of a stochastic signal are obtained by computing the Fourier transform of the autocorrelation function [33].

Consider a noiseless, jitterless received signal $r_N(t)$ given by Equation (1.1). We assume that the sequence $a_n \epsilon \left\{0, 1\right\}$ is statistically independent and equiprobable. The mean of $r_N(t)$ is

$$E\left\{r_N(t)\right\} = E\left\{a_N\right\} \sum_{n=-\infty}^{\infty} g_N(t-nT) \qquad \ldots(2.1)$$

and its autocorrelation is

$$R_{rr}(t,t+\tau) = E\left\{r_N(t)r_N^*(t+\tau)\right\}$$, where $r_N^*(t)$ is the complex conjugate of $r_N(t)$.

$$= E\left\{ \sum_{n=-\infty}^{\infty} a_n g_N(t-nT) \sum_{k=-\infty}^{\infty} a_k \; g_N(t-kT+\tau) \right\} \qquad \ldots(2.2)$$

$$= E\left\{ \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} a_n a_{n+m} \; g_N(t-nT) \; g_N(t-nT-mT+\tau) \right\} \qquad \ldots(2.3)$$

where $k=n+m$

$$= \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} E\left\{a_n a_{n+m}\right\} g_N(t-nT) \; g_N(t-nT-mT+\tau) \qquad \ldots(2.4)$$

It is seen that both the mean and the autocorrelation of $r_N(t)$ are periodic with T. A stochastic process with a periodic mean and autocorrelation is referred to as *cyclostationary* [27]. Because $r_N(t)$ is cyclostationary with period T, a timing signal with period T can be extracted from it [34].

The time dependence of $R_{rr}(t,t+\tau)$ can be eliminated by averaging over the period T. This results in an average autocorrelation

$$\bar{R}_{rr}(\tau) = \frac{1}{T}\int_{-T/2}^{T/2} R_{rr}(t,t+\tau)\ dt \qquad \ldots(2.5)$$

$$= \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} E\left\{a_n a_{n+m}\right\} \frac{1}{T}\int_{-T/2-nT}^{T/2-nT} g_N(t)\ g_N(t-mT+\tau)\ dt \qquad \ldots(2.6)$$

Since a_n is wide-sense stationary, $E\left\{a_n a_{n+m}\right\}$ does not depend on n;

$$\text{therefore } \bar{R}_{rr}(\tau) = \sum_{m=-\infty}^{\infty} E\left\{a_n a_{n+m}\right\} \frac{1}{T}\int_{-\infty}^{\infty} g_N(t)g_N(t-mT+\tau)\ dt \qquad \ldots(2.7)$$

By defining $R_{gg}(\tau) = \int_{-\infty}^{+\infty} g_N(t)\ g_N(t+\tau)\ dt$ and $R_{aa}[m] = E\left\{a_n a_{n+m}\right\}$

...(2.8)

and substituting in equation (2.7), we have

$$\bar{R}_{rr}(\tau) = \frac{1}{T}\sum_{m=-\infty}^{\infty} R_{aa}[m]\ R_{gg}(\tau-mT)$$

$$= \frac{1}{T}\ R_{gg}(\tau) * \sum_{m=-\infty}^{\infty} R_{aa}[m]\ \delta(\tau-mT) \qquad \ldots(2.9)$$

Fourier transforming (2.9) yields the average power spectrum of $r_N(t)$

as $$\bar{S}_{rr}(f) = \frac{1}{T}\ |G_N(f)|^2\ S_{aa}(f) \qquad \ldots(2.10)$$

where $G_N(f)$ is the Fourier transform of $g_N(t)$, and $S_{aa}(f)$ is the power spectrum of the message sequence $\{a_n\}$ defined as

$$S_{aa}(f) = \sum_{m=-\infty}^{\infty} R_{aa}[m]\, e^{-j2\pi f m T} \qquad \ldots(2.11)$$

Equation (2.10) shows that the average power spectrum of $r_N(t)$ is dependent on the pulse shape and the statistics of the message sequence. The effect of message sequence statistics will be examined first for two cases.

CASE I: If the message sequence, $\{a_n\} \in \{0,1\}$ is independent and equiprobable, then from equation (2.8), the autocorrelation of a_n is $R_{aa}[m] = 1/4\ \delta[m] + 1/4$ and

$$S_{aa}(f) = \frac{1}{4} + \frac{1}{4T} \sum_{m=-\infty}^{\infty} \delta\left[f - \frac{m}{T}\right] \qquad \ldots(2.12)$$

Substituting (2.12) in (2.10) yields an average power spectrum of the received signal $r_N(t)$ of

$$\bar{S}_{rr}(f) = \frac{1}{4T} \left|G_N(f)\right|^2 + \frac{1}{4T^2} \sum_{m=-\infty}^{\infty} \left|G_N\left(\frac{m}{T}\right)\right|^2 \delta\left[f - \frac{m}{T}\right] \qquad \ldots(2.13)$$

Therefore, for an independent message sequence, $\bar{S}_{rr}(f)$ has a continuous spectrum of just the pulse shape magnitude squared plus discrete components at $f = m/T$.

CASE II: If the message sequence has some periodicity, such as a bit sequence produced by a shift register pattern generator, $R_{aa}[m]$ will be periodic, with period υ bits [94]. The autocorrelation of a_n then becomes, from equation (2.8),

$$R_{aa}[m] = 1/4\ (1+1/\upsilon)\ \delta[m] + 1/4\ (1-1/\upsilon) \qquad \ldots(2.14)$$

for $m = 0$ to υ and $R_{aa}[m+k\upsilon] = R_{aa}[m]$, for all integer values of k. Inserting (2.14) into (2.11) yields

$$S_{aa}(f) = \frac{1}{4}(1+1/\upsilon)\sum_{k=-\infty}^{\infty}\delta\left[f-\frac{k}{\upsilon T}\right] + \frac{1}{4T}(1-1/\upsilon)\sum_{m=-\infty}^{\infty}\delta\left[f-\frac{m}{T}\right] \qquad \ldots(2.15)$$

Substituting (2.15) into (2.10) yields an average power spectrum of the received signal $r_N(t)$ of

$$\bar{S}_{rr}(f) = \frac{1}{4T}(1+1/\upsilon)\sum_{k=-\infty}^{\infty}\left|G_N\left(\frac{k}{\upsilon T}\right)\right|^2 \delta\left[f-\frac{k}{\upsilon T}\right]$$

$$+ \frac{1}{4T^2}(1-1/\upsilon)\sum_{m=-\infty}^{\infty}\left|G_N\left(\frac{m}{T}\right)\right|^2 \delta\left[f-\frac{m}{T}\right] \qquad \ldots(2.16)$$

Therefore, for a periodic shift register pattern, $\bar{S}_{rr}(f)$ has a discrete spectrum with impulses at $f_k = k/\upsilon T$. The magnitudes of the impulses are shaped by the pulse shape magnitude squared.

In the limit as υ tends to infinity equation (2.16) reduces to (2.13). In other words, the spectrum of a periodic message sequence consists of impulses spaced $1/\upsilon T$ Hz apart and as υ tends to infinity this portion of the power spectrum becomes a continuum. Cases I and II illustrate the effect of the message statistics on the received signal's power spectrum.

To limit the intersymbol interference, and therefore the probability of error, a raised cosine pulse shape from the Nyquist family is chosen, having a transform

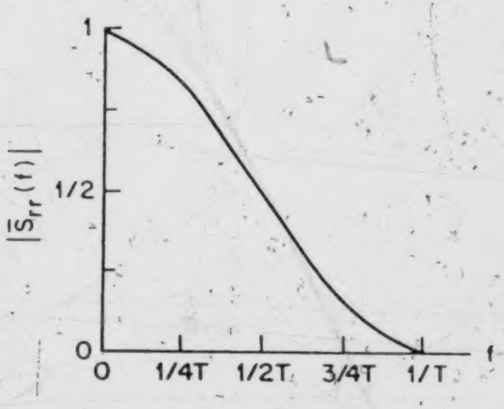
$$G_N(f) = T/2 \left[1 - \sin \pi T\left(f - 1/2T\right)\right] \qquad , \; 0 < f < 1/T$$

Figure 2.1 shows the plot of equation (2.10) using the above $G_N(f)$ for an independent message signal (2.13) and for a periodic message signal (2.16). We see that for both cases, there is no power at the bit repetition frequency 1/T, although we know that a timing signal exists since $r_N(t)$ is cyclostationary with period T. To extract a timing signal, the received signal should be subjected to some nonlinear operation, as explained in the next section.

2.3 Timing Extraction

The received pulse trains cannot be used directly as timing signals, since they still do not contain pulses in every time slot and further operations are needed to generate a repetitive train of clock pulses. The received data signal is first applied to a non-linear circuit and then to a clock recovery circuit. The output of the clock recovery circuit is used to sample the received signal. The block diagram of such a self synchronization scheme is shown in Figure 2.2.

The non-linear element generates a discrete tone at the symbol rate frequency [3]. If a spectral line already exists in the line code, e.g. RZ, CMI or Manchester codes, then the non-linear element is omitted. The non-linear element essentially converts the negative transitions in the input signal into positive ones, thus producing a signal that has positive transitions at integral multiples of the bit period T, which will give rise to a discrete spectral component at the desired bit rate of 1/T. The non-linear function may be implemented by various techniques, such as a delay-and-multiply bit synchronizer [35], a full-wave rectifier [27], a squarer [36,37], a threshold crossing



INDEPENDENT MESSAGE SEQUENCE

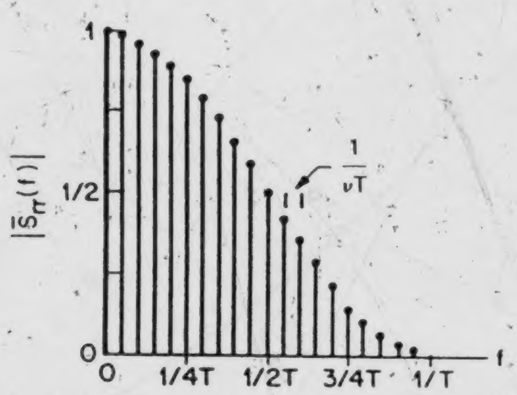


Fig. 2.1 Average Power Spectrum of the Received Signal with [2]
(a) Independent Message Sequence and
(b) Periodic Message Sequence

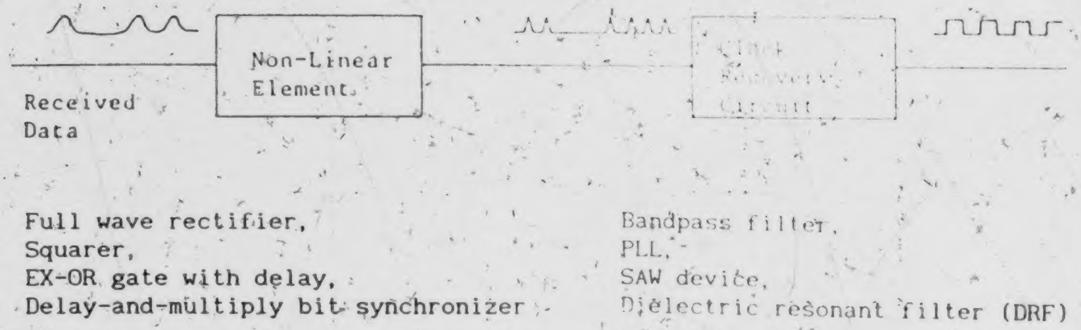

Non-Linear Element
Received Data
Clock Recovery Circuit
Full wave rectifier,
Squarer,
EX-OR gate with delay,
Delay-and-multiply bit synchronizer
Bandpass filter,
PLL,
SAW device,
Dielectric resonant filter (DRF)

Fig.2.2 Block Diagram of the Timing Extraction Circuit Using the Self-synchronization Scheme

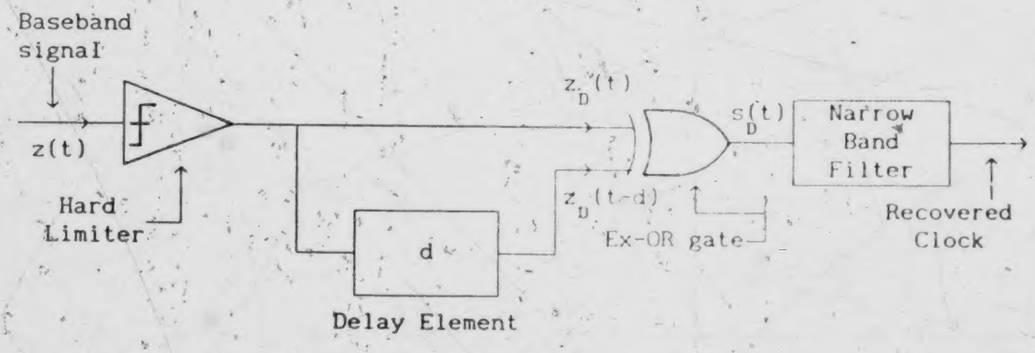

Baseband signal
z(t)
Hard Limiter
$z_D(t)$
$z_D(t-d)$
d
Delay Element
Ex-OR gate
$s_D(t)$
Narrow Band Filter
Recovered Clock

Fig.2.3 Timing Extraction Circuit [40]

circuit [38], a fourth-power circuit [39], or an Exclusive-OR circuit [40-44].

The clock recovery circuit is generally an LC bandpass filter, a phase-locked-loop (PLL) [45], a high-Q surface-acoustic-wave (SAW) filter [37], or a dielectric resonant filter (DRF) [35,46] tuned to the pulse repetition frequency. It has been reported that a high gain, second-order PLL is superior to an LC filter for timing extraction [45,47]. A PLL is advantageous because it has a constant output amplitude, whereas the output of a bandpass filter is a function of its input bit sequence. In the absence of pulses at the input, the output will decay exponentially at a rate that is inversely proportional to the Q of the filter [5]. Also, in a PLL, the static phase error and noise bandwidth can both be made small at the same time. In a bandpass filter, a small static phase error is possible only if the noise bandwidth is increased, i.e. its Q is decreased [48]. The SAW filter has the advantage of high Q but also has a high insertion loss. The dielectric resonator filter (DRF) has been used at extremely high data rates both, since the PLL and a SAW filter are difficult to implement at very high frequencies [46].

In this thesis, an Exclusive-OR gate was used as the non-linear element in order to generate a discrete spectral line at the signalling rate. The timing extraction circuit is shown in Figure 2.3. As shown in this figure, the received baseband signal z(t) is converted to a binary data stream using the hard-limiter [40,49,50]. The binary data stream $z_D(t)$ resembles an NRZ signal. The spectrum of $z_D(t)$ does not contain any discrete spectral lines. To obtain a modified return-to-zero (RZ) signal which does contain a discrete spectral component at the signalling frequency 1/T, the signal $z_D(t)$ and its delayed version $z_D(t-d)$ (where $0 < d < T$) are passed through an Exclusive-OR gate. The clock is then extracted by employing a narrow bandpass filter centered at the signalling frequency.

The random signal $z_D(t)$ is represented as

$$z_D(t) = \sum_{n=-\infty}^{\infty} z_n \, g(t-nT) \qquad \ldots (2.17)$$

where $z_n = a$, or 0 with probability 1/2 and

$$g(t-nT) = \begin{cases} 1, & nT < t \leq (n+1)T \\ 0, & \text{elsewhere.} \end{cases}$$

The power spectrum $Sz_D(f)$ of equation (2.17) is given by [91] as

$$Sz_D(f) = (a^2/4) \, . \, T \, . \, \mathrm{sinc}^2 (\pi f T) \qquad \ldots (2.18)$$

which is shown in Fig. 2.4. As can be noted from Fig. 2.4, there are no discrete spectral lines at the symbol rate frequency which can be extracted for synchronization purposes.

The output of the Exclusive-OR gate $s_D(t)$ is

$$s_D(t) = \sum_{n=-\infty}^{\infty} s(t-nT) \qquad \ldots (2.19)$$

where $$s(t-nT) = \begin{cases} h_1(t-nT) & \text{with probability } 1/2 \\ h_2(t-nT) = 0 & \text{with probability } 1/2 \end{cases}$$

and $$h_1(t-nT) = \begin{cases} a, & nT < t \leq (nT + d) \\ 0, & (nT + d) < t \leq (n + 1)T \end{cases}$$

The power spectral density of $s_D(t)$ is given by [91]

$$S_{sD}(f) = (1/2T) \, |H_1(f) - H_2(f)|^2 + (1/4\,T^2) \, |H_1(0) + H_2(0)|^2 \, \delta(f) \, +$$

$$(1/2T^2) \, . \sum_{m=1}^{\infty} |H_1(m/T) + H_2(m/T)|^2 \, \delta(f - m/T) \qquad \ldots (2.20)$$

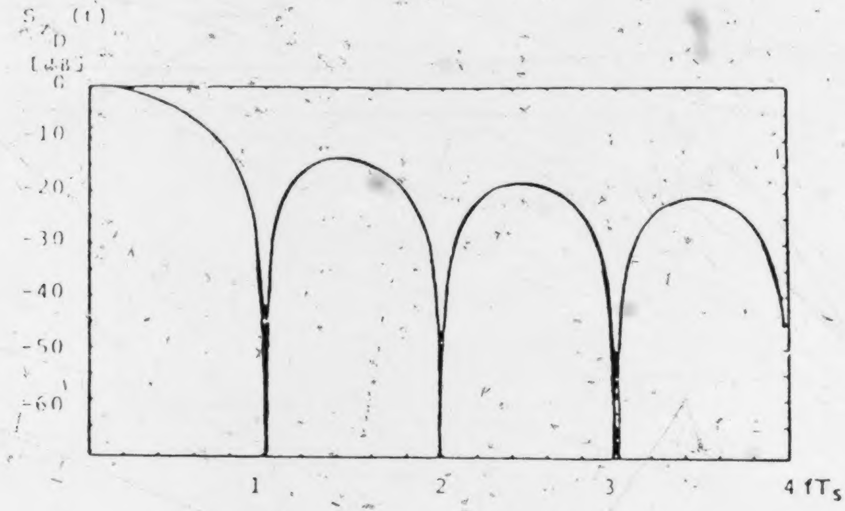


Fig. 2.4 Power Spectrum of $z_D(t)$ [40]

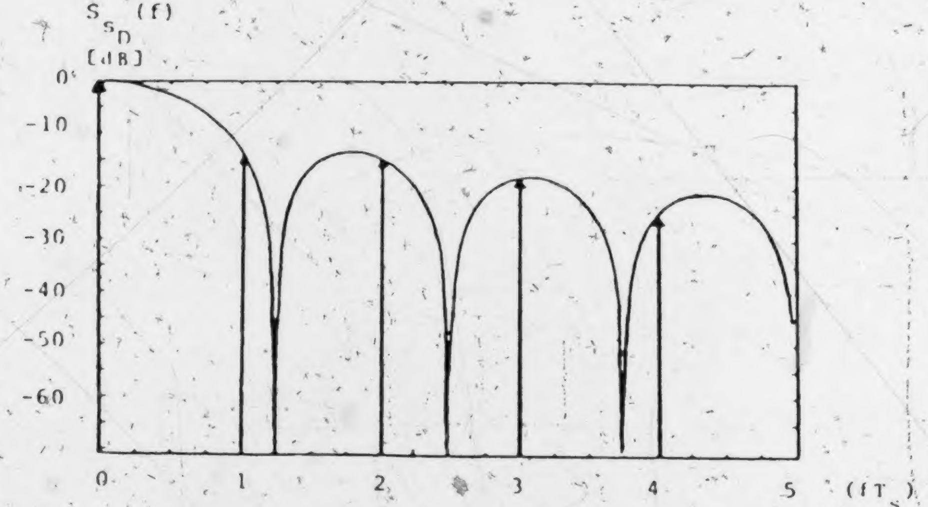


Fig. 2.5 Power Spectrum of $s_D(t)$ [40]

where
$$H_1(f) = \int_{-\infty}^{+\infty} h_1(t)\, e^{-j2\pi ft}\, dt$$

$$= ad\ \mathrm{sinc}(\pi fd)\ e^{-j\pi fd} \qquad \ldots(2.21a)$$

and
$$H_2(f) = \int_{-\infty}^{+\infty} h_2(t)\, e^{-j2\pi ft}\, dt = 0 \qquad \ldots(2.21b)$$

Substituting (2.21a), (2.21b) into (2.20), the power spectral density at the output of the Exclusive-OR gate becomes

$$S_{sD}(f) = (2a^2 d^2 / T)\ \mathrm{sinc}^2\ (\pi fd) + (a^2 d^2 / T^2)$$
$$.\left[\delta(f) + 2\sum_{m=1}^{\infty} \mathrm{sinc}^2 \left(\frac{m\pi d}{T}\right) . \ \delta(f - m/T)\right] \qquad \ldots(2.22)$$

and is shown in Fig. 2.5.

A delay $d = T/2$ yields the maximum power of the discrete spectral line at the symbol rate frequency [38,40,49]. However, this does not guarantee the optimum performance. The best performance is determined by the *ratio of the discrete to residual continuous spectral power*, since it is this ratio which determines the amount of jitter on the recovered clock. The discussion which follows proves that this power ratio is equal to the quality factor Q of the narrow band filter, centered at the signalling frequency.

From equation (2.22) the power contained in the discrete spectral line at 1/T is given by

$$D(1/T) = (2\ a^2\ d^2 / T^2) .\ \mathrm{sinc}^2(\pi d/T) \qquad \ldots(2.23)$$

The residual power contained in the continuous part of $S_{sD}(f)$, which falls within the bandwidth of the narrow band filter contributes to the timing jitter. Assuming that the filter has a very narrow bandwidth, so that the continuous spectrum is flat within the bandwidth, the power contained in the continuous part is given by (from equation (2.22))

$$C(1/T) = BW\,.\,(2\,a^2\,d^2/\,T)\,.\,\mathrm{sinc}^2(\pi d/T) \qquad \ldots(2.24)$$

The signal-to-noise ratio in the bandwidth BW is then given by

$$(SNR)_{BW} = D(1/T)\,/\,C(1/T) = 1/\,(BW.T) = Q \qquad \ldots(2.25)$$

Thus, it is the quality factor Q of the filter which determines the output jitter rather than the delay time d of the non-linear element.

2.4 Accumulation of Timing Jitter

Timing jitter will arise from several sources in digital line links consisting of self-timed regenerator sections connected in tandem. Random sources of jitter such as noise and crosstalk will, in general, be present in each regenerator section but will be *uncorrelated*. Thus, the resulting jitter falling within the bandwidth of the regenerator timing recovery circuits will accumulate on a *power basis*. The predominant source of jitter in each regenerator section is usually the pulse pattern sensitivity of the regenerator timing recovery circuits; jitter from sources of this type, known as *pattern induced* or *systematic jitter*, will occur in phase in each regenerator section or in otherwords will be *correlated*, because the same pulse pattern passes through all the regenerators. These cumulative components will add on an *amplitude basis* [54].

Since noise-dependent jitter is uncorrelated with that generated by the other regenerators in the chain, this jitter will accumulate randomly. The pattern-dependent jitter will accumulate systematically since it is correlated with the jitter generated by the other regenerators in the chain. The random jitter generated in each regenerator is assumed as a zero-mean, white stochastic process. For a chain of **N** cascaded nonidentical regenerators the **rms** value of the accumulated random jitter at the end of the chain is [2]

$$\sigma_R[N] = \sqrt{\int_{-1/T}^{1/T} \phi_N^R(f)\, df} \qquad \ldots(2.26)$$

where $\phi_N^R(f)$ is the random jitter power spectral density at the end of the chain for $|f| < 1/T$.

Assuming that the systematic jitter generated at each regenerator is a zero-mean, white stochastic process, the **rms** values of the accumulated systematic jitter at the end of a chain of **N** cascaded nonidentical regenerators is [2]

$$\sigma_s[N] = \sqrt{\int_{-1/T}^{1/T} \phi_N^s(f)\, df} \qquad \ldots(2.27)$$

where $\phi_N^s(f)$ is the systematic jitter power spectral density at the end of the chain for $|f| < 1/T$.

Since random and systematic jitter are uncorrelated, the total jitter power spectrum $\phi_N(f)$, and the total rms jitter $\sigma[N]$, at the output of the **Nth** cascaded regenerator, are

$$\phi_N(f) = \phi_N^R(f) + \phi_N^S(f) \qquad \ldots(2.28)$$

and

$$\sigma[N] = \sqrt{\sigma_R^2[N] + \sigma_S^2[N]} \qquad \ldots(2.29)$$

In particular, in repeatered digital line transmission systems with identical repeaters, random jitter accumulates with an amplitude proportional to the fourth-root of the number of repeaters and systematic jitter accumulates with an amplitude proportional to the square-root of the number of repeaters [28,29,54].

The current trend towards higher-capacity optical links has placed increased emphasis on system verification with respect to jitter accumulation prior to installation. Jitter accumulation is particularly important on trans oceanic routes which contain many repeaters. A number of jitter accumulation measurement experiments have been reported which feature either cascaded electrical or looped optical regenerators [51-62].

2.5 Effect of Jitter on Transmission Quality

The performance of an optical communication system depends critically on the signal-to-noise ratio (SNR) of the transmitted signal at the receiver. Timing jitter causes the decision point, nominally set at the bit centre, to fluctuate around its mean value. This variation of the sampling time can lead to performance degradation if the jitter occurs over a significant fraction of the bit period.

A correct bit decision is not dependent on the magnitude of the input nor the output jitter but the difference between the two (i.e. the alignment jitter). Added to this, a correct bit decision depends on several other factors such as the shot noise, thermal (circuit) noise, laser noise, received pulse shape, the decision threshold, the bit sequence before and after the present bit decision and the static phase offset. As a result there is a power penalty, associated with time jitter.

The origin of power penalty due to time jitter is as follows. Because of decision-time fluctuations, different portions of the received waveform are sampled from bit to bit. Resulting signal fluctuations generate additional noise and degrade the SNR. To maintain the same SNR, the average received power should be increased. The relative increase in the received power is referred to as the *power penalty*. The power penalty depends on the received waveform being sampled by the decision circuit. The received waveform in turn depends on the transmitter through relaxation oscillations, frequency chirping etc., the dispersion of the fiber, and on the receiver through the equalizer, filter etc.[63].

As the probability of making a correct bit decision depends on the decision threshold, DC offsets in the sampling portion of the decision circuit should be minimized. Ideally, a sampling threshold of V=0 is selected. A static phase offset is caused by the physical separation of the timing and decision circuits. This static phase alignment between the data and the timing signals is set by choosing the length of a coaxial cable between the timing and decision circuits such that the data signal is sampled at an optimum time.

It is reported that [2], with no alignment jitter, the effect of optimum static phase on transmission performance is small. A power penalty of less than 0.5 dB occurs for static phase offsets as large as 34° (bit period $T=360^\circ$) from the optimum with zero alignment jitter. However when alignment jitter is present, static phase offset becomes important. The regenerator becomes less tolerant of accumulated alignment jitter when static phase offset is present. Thus, the static phase offset must be minimized in order to minimize the effect accumulated alignment jitter has on the probability of error P_e. The performance degradation of optical communication systems due to jitter could be evaluated by assuming different probability distributions for the alignment jitter. It is reported, that depending on the approximation, we may either under- or over- estimate the performance degradation by a significant amount [64]. Sinusoidal alignment jitter results in power penalties that are about one dB larger than those caused by truncated Gaussian distribution [2]. Timing jitter also affects the system performance by degradation of the measured receiver sensitivity. It lowers the optical gain of the avalanche photodiodes and will reduce the improvement in receiver sensitivity of using avalanche photodiodes over PIN detectors [65].

The performance of a heterodyne M-PSK coherent optical fiber communication system has been investigated with respect to the time jitter [66]. The extent of degradation due to time jitter was almost the same for all values of M, for a fixed jitter variance. The power-penalties show a sharp rise above a certain threshold value of time jitter, irrespective of the value of M. The time jitter thus does not affect the choice of the order of the system. The performance of a digital communication system is usually shown by the curves of bit error rate (BER) versus SNR with constant values of jitter variance as a parameter [67,68]. However, in any real practical system, the variance consists of a relatively small constant component (σ_c^2) and a component which is inversely proportional to the SNR (σ_n^2). Hence the curves of BER versus SNR with variance ($\sigma^2 = \sigma_c^2 + \sigma_n^2$) as a parameter are more realistic [69].

In the next chapter we discuss in detail, the operation of the self-sustaining monostable multivibrator clock recovery circuit which has been used in this thesis.

CHAPTER 3

THE SELF-SUSTAINING MONOSTABLE MULTIVIBRATOR CLOCK RECOVERY CIRCUIT

A novel clock recovery circuit using a self-sustaining monostable multivibrator, shown in Figure 3.1, was reported by Witte and Moustakas [70]. This timing extraction device is very attractive because it is simple to implement, inexpensive and, since it is digital, can be constructed using logic gate array technology. Furthermore, this clock recovery circuit is not restricted to the NRZ code with a scrambler (the application reported in [70]), it can also be used with any other line code that has a reasonable restriction placed on the number of consecutive ones and zeros allowed; e.g., simple 1B-2B codes, such as the Petrovic [14], CMI, DMI and Miller. The original paper on this clock recovery circuit concentrates on the circuit operation and gives an equation for determining the maximum number of consecutive ones or zeros allowed in the input signal for proper operation. It also gives experimental verification of the circuit operation for a 16 Mb/s fiber-optic local area network employing NRZ signalling with a scrambler. However, the original clock recovery circuit does not adequately suppress the jitter in the incoming data stream, resulting in an increased BER at low values of signal-to-noise ratio. Subsequently, a modified clock recovery circuit, which significantly reduces the jitter present in the output signal, was proposed and implemented in an experimental fiber optic system using the Petrovic code [5].

In this project, the high frequency jitter performance of the self-sustaining monostable multivibrator clock recovery circuit is examined more rigorously on a bit-by-bit basis. It has been implemented in an experimental fiber optic system employing NRZ

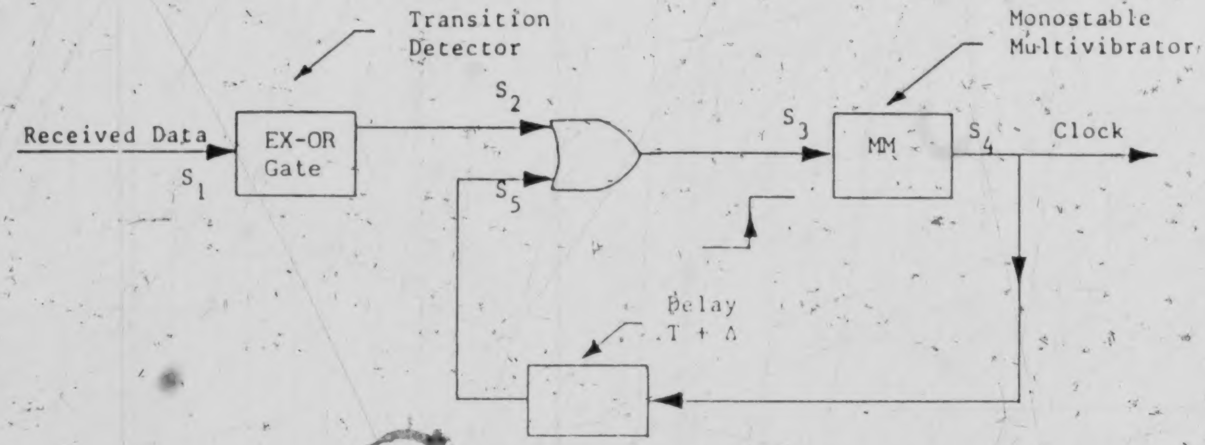

Transition
Detector
Monostable
Multivibrator
Received Data
S_1
EX-OR
Gate
S_2
S_5
S_3
MM
S_4
Clock
Delay
T + Δ

Fig. 3.1 The Self-Sustaining Monostable Multivibrator Clock Recovery Circuit [70]

signalling without a data scrambler.

3.1 Circuit Operation

A timing diagram of the self-sustaining monostable multivibrator clock recovery circuit is shown in Figure 3.2 (from [70]). For the sake of simplicity, it is assumed here that the propagation delay of all the gates and of the monostable multivibrator (MM) is zero between their respective inputs and outputs. In order to understand the operation of the circuit, consider the circuit response, after being turned on, to the input bit sequence 10001, waveform S1 in Figure 3.2. (S1 is obtained directly from the receiver output). The transition detector generates a pulse on every rising and falling edge of the input signal, as shown by S2 in Figure 3.2. (Referring to Figure 2.2 in Section 2.3, the transition detector constitutes the non-linear element which is required to generate the clock spectral line). The width of these pulses is equal to the delay T_P and is not a critical design parameter [40], as long as it is of sufficient duration to trigger the MM. In Figure 3.2, T_P is arbitrarily chosen to be T/5, where T is the bit interval. A monostable multivibrator with a feedback path around it follows the transition detector. The MM produces a pulse on every rising edge of its input (S4). It can be triggered by the pulses generated by the transition detector, here referred to as the primary pulses, or by the feedback pulses (S5 in Figure 3.2). The feedback delay T1 is chosen to be slightly greater than T; i.e., $T1 = T + \Delta$, where Δ is a small positive quantity. Thus, the feedback pulse triggers the MM only when the primary pulse is missing (or late). In practice, Δ is chosen to be as small as possible. The third and fourth bit interval of the input signal shown

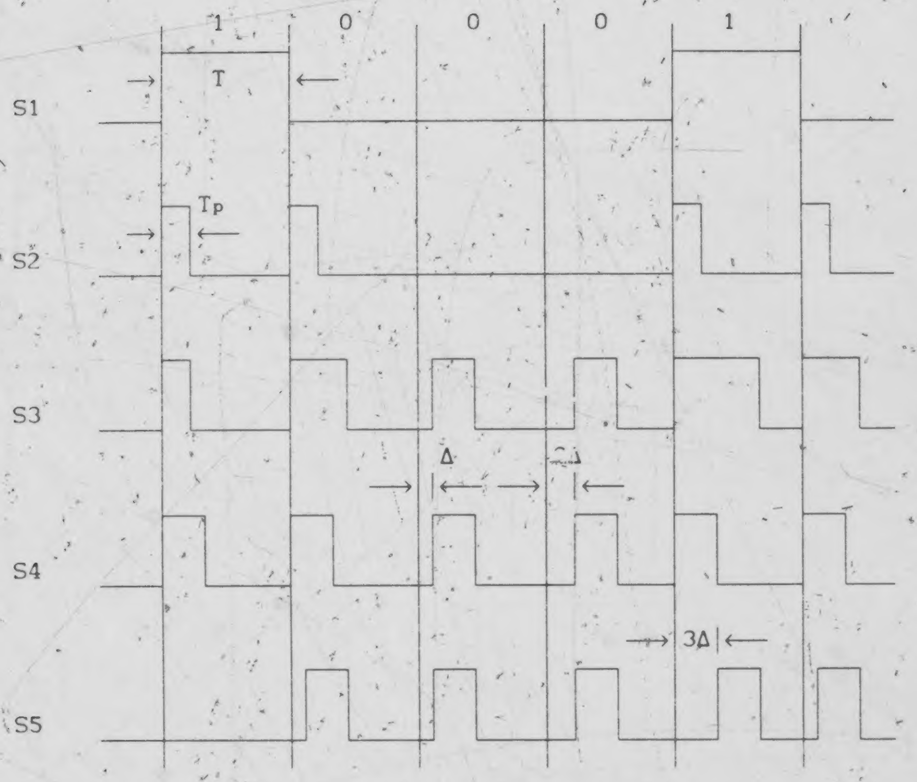

1
0
0
0
1
T
S1
Tp
S2
S3
Δ
2Δ
S4
3Δ
S5

Fig. 3.2 Timing Diagram of the Self-Sustaining Monostable Clock Recovery Circuit for a 10001 Input Bit Sequence

in Figure 3.2 do not contain transitions. Hence, the transition detector does not produce a pulse during these intervals. In this situation, the feedback pulse triggers the MM to produce the clock pulse Δ seconds after the ideal time for the third bit interval and 2Δ seconds after the ideal time for the fourth bit interval. In the fifth bit interval, a transition from a 0 to 1 occurs in the input bit stream and hence a primary pulse triggers the MM at the ideal time. Thus, we see that, when a long sequence of zeros or ones occur in the input, the clock signal advances in time by Δ seconds during each bit interval until a transition occurs. This is a simplified description of the circuit operation and is valid only when the signal jitter is negligible; the effect of jitter will be considered in the next section.

The feedback delay must not be less than the bit interval T. If this is not so, the positive edges of S4 will not coincide with the input bit transitions. As a result, the clock will drift out of phase (oscillates at a frequency of 1/T1) and synchronization will never be attained. The maximum number of consecutive ones or zeros that can occur in the input with synchronization still being maintained is determined by how small Δ can be made; i.e., how closely T1 approximates T, but with the restriction T1 > T. This minimum depends on the variation of propagation delays of the logic gates and the delay network with temperature.

In addition, the recovery time of the MM, Tr, affects the maximum interval between transitions by limiting the maximum possible phase shift. The recovery time of the MM is defined as the time required by the MM, after its output has returned to the stable state, before it can be triggered again. The maximum possible phase shift that is allowed is $T-T_m-T_r$, where T_m is the MM output pulse width. Thus, the maximum number of consecutive ones or zeros allowed in the input bit stream, N, is [70]:

$$N = 1 + (T - T_m - T_r)/\Delta \qquad \ldots(3.1)$$

The "1" in the above equation accounts for the fact that the first bit in the input has already been received before the MM output begins to drift out of phase. From this equation, we see that, for high bit-rate operation (i.e., small values of T), T_m and T_r should be made as small as possible. Also, notice that, for fixed values of T, T_m and T_r, the value of Δ increases as the number of consecutive ones or zeros in the input signal, N, decreases. It is advantageous to make N small, since it is easier to construct a delay network that provides a delay of $T+\Delta$ seconds for large values of Δ than for small values of Δ. Thus, implementation of this clock recovery circuit is easier for line codes that have a reasonable restriction placed on the number of consecutive ones or zeros which may occur. In this project, although we used an NRZ code without a data scrambler, the number of consecutive ones or zeros which may occur could be preset in the data generator.

3.2 Jitter Generated in a Self-Sustaining Monostable Multivibrator Clock Recovery Circuit

In the ideal case with zero input jitter, the pulses generated by the transition detector, referred to as primary pulses, trigger the MM at integral multiples of the bit interval T. In practice, the arrival times of the primary pulses will fluctuate or *jitter* around the ideal arrival times nT. The jitter in the threshold crossings of the primary pulses is assumed to have a zero-mean Gaussian probability density function (pdf) with a variance σ_1^2. Regenerators in digital systems generally experience a Gaussian jitter distribution at their input [2,72]. Figure 3.3 shows how the bit transition jitter is generated due to the effect of the noise. Ideally, the received signal will cause the gate to trigger at exact multiples of T seconds (= bit period). However, due to the noise contained in the input signal, the threshold crossings will deviate from the ideal times. Ideally it should cross at t_o, but due to noise it actually crosses at t_1. The difference $t_o - t_1$ is the bit transition jitter $j_1(t)$ which is present at the input of the clock recovery circuit. Following [41] we have,

$$j_1(t) = n(t)/\text{ Slope of the signal}$$
$$= t_r\, n(t)/A \qquad \ldots(3.2)$$

where t_r = rise time of the input signal

$n(t)$ = receiver noise characteristic

A = amplitude of the logic gate output in the high state

Thus, the jitter is a function of the receiver noise characteristics and is directly proportional to the rise time t_r of the input signal. In addition, the jitter variance depends on the channel and receiver bandwidth, received optical pulse shape, type of line coding used, received optical power, comparator threshold level etc.

Let us next determine the output jitter pdf of the self-sustaining monostable multivibrator clock recovery circuit for a Gaussian input jitter pdf. For the sake of clarity, it is assumed that the delay of the gates and of the MM can be neglected. Assume that initially a primary pulse triggers the MM at the ideal time (i.e. $j_1(t) = 0$), causing the delayed output pulse to arrive at the OR gate of Figure 3.1 $T+\Delta$ seconds later. If the input jitter $j_1(t) < \Delta$, then the primary

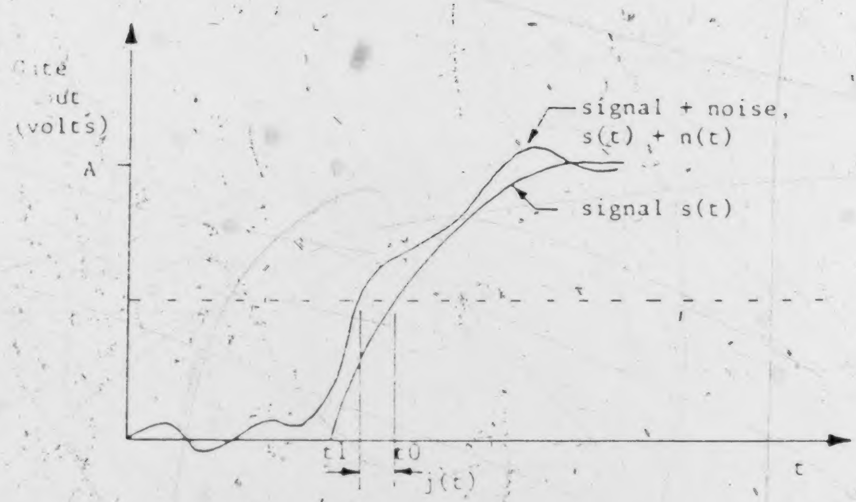

Gate
Out
(volts)
A
signal + noise,
s(t) + n(t)
signal s(t)
t1
t0
j(t)
t

Fig. 3.3 Relationship Between Jitter, j(t), and Receiver Noise, n(t), when the Received Signal is first applied to a Logic Gate [5]

pulse will trigger the MM because it reaches the OR gate before the delayed output pulse. In this case, the output pulse will occur $j_i(t)$ seconds away from the ideal time and hence the output jitter $j_o(t)$ will be equal to $j_i(t)$. On the other hand, if $j_i(t) > \Delta$, then the delayed output pulse will trigger the MM and $j_o(t)$ will be equal to Δ, irrespective of the value of $j_i(t)$. Note that the feedback loop has prevented any primary pulse arriving Δ seconds or more after the ideal time from triggering the MM. The output jitter pdf for this case is shown in Figure 3.4. An impulse exists at $t=\Delta$ to ensure that the area under the Probability distribution function (PDF) is equal to unity [73]. The ratio of the input jitter variance to the output jitter variance, σ_0^2/σ_i^2, for $\Delta = \sigma_i/10$ is equal to 0.505 [74].

Although the input jitter has a zero mean, the output jitter pdf will have a non-zero mean. As the value of Δ increases, the output jitter increases and hence the value of the ratio σ_o^2/σ_i^2 increases. The output jitter pdf is not time independent. When primary pulses are missing or late, the MM is triggered by the feedback signal. In such a case the pdf extents to the right by Δ seconds for each missing primary pulse. For example, if a primary pulse is missing and the delayed output pulse triggers the MM Δ seconds after the ideal arrival time, then the output jitter pdf for the next bit interval will be as shown in Figure 3.5. Thus an exact average for σ_o^2/σ_i^2 will be difficult to evaluate. However, if $\Delta \ll \sigma_i$, it can be seen intuitively that the average value of σ_0^2/σ_i^2 will be approximately equal to 0.5 [74]. The value of Δ cannot be less than zero, otherwise the MM clock recovery circuit will self-oscillate [illegible] a frequency of 1/T+Δ Hz [5]. The smallest value of Δ is limited, in practice, by the tolerance on

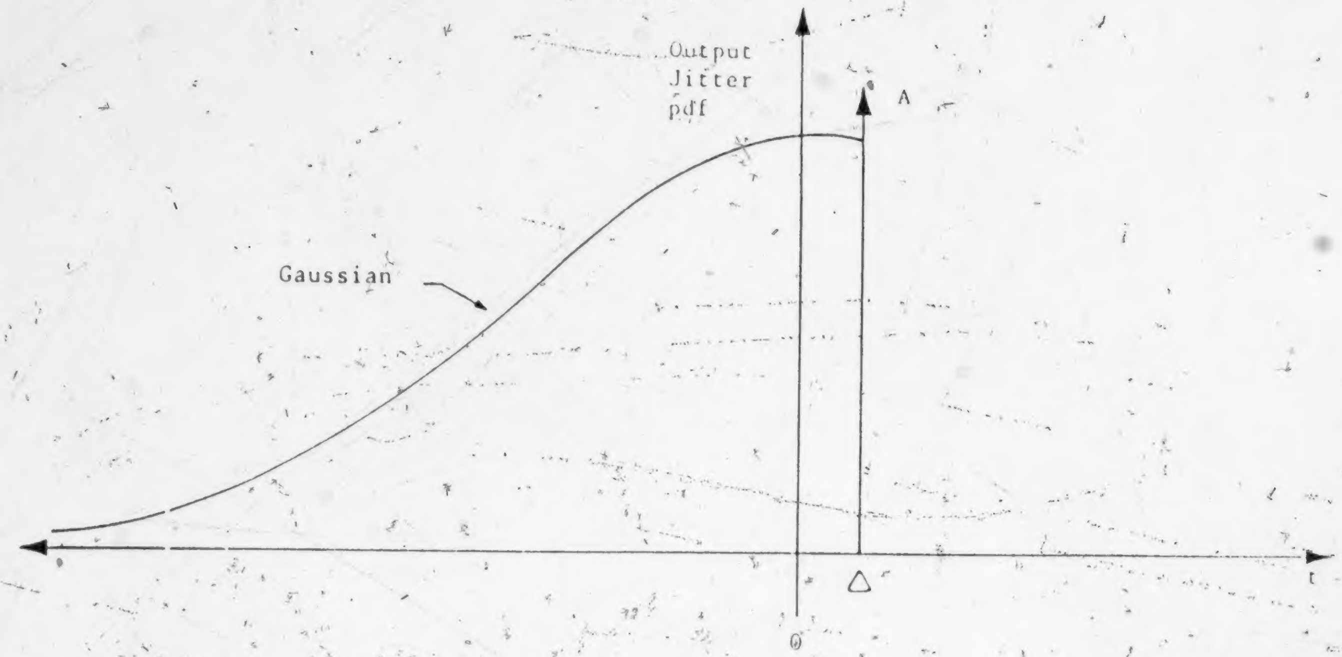


Fig. 3.4 Pdf of Output Jitter when a Primary Pulse Triggers the MM at the Ideal Time during the Previous Time Slot [5]

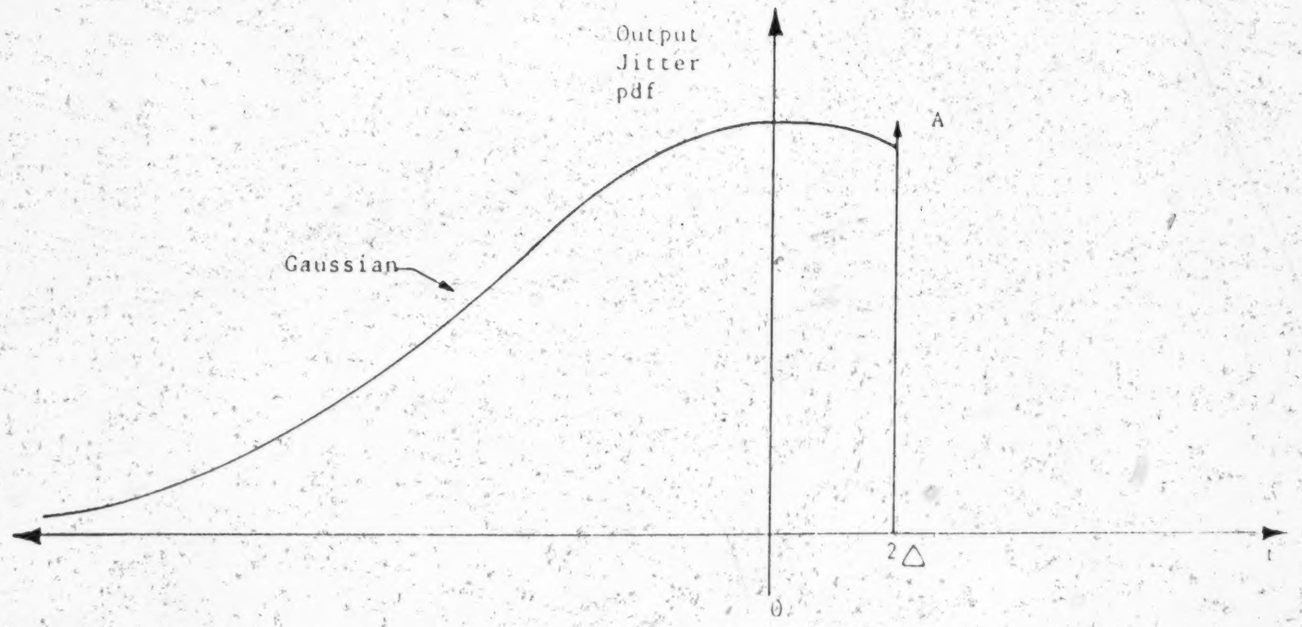


Fig. 3.5 Pdf of Output Jitter when a Feedback Pulse Triggers the MM at Δ Seconds after the Ideal Time during the Previous Time Slot [5]

the incoming signal bit-rate, and possible variations in the time delays associated with the MM circuit.

3.3 Modified Monostable Clock Recovery Circuit

Recently, a modified MM clock recovery circuit was proposed by Visvanatha [74], in order to reduce the output jitter in the recovered clock. A substantial reduction in the output jitter variance will occur if early primary pulses were inhibited from triggering the MM as well as the late arriving ones. If all the primary pulses that arrive earlier than Δ' seconds before the ideal time are made to trigger the MM only Δ' seconds early and the late pulses are inhibited as before, then the output jitter PDF will take the form shown in Figure 3.6 (for the case when a primary pulse triggers the MM in the previous time slot with $j_1(t) = 0$). If $\Delta' = \Delta = \sigma_1/10$, then $\sigma_0^2/\sigma_1^2 = 0.01027$, which is approximately 50 times less than when the early primary pulses are not inhibited [74]. Here too, it was observed that when Δ' was less than 0.1 ± 0.01ns, the modified clock recovery circuit lost synchronization with the transmitter clock [5]. Thus we note that there exists a minimum width of the window $(\Delta - \Delta')$ for proper operation of the clock recovery circuit.

Primary pulses that arrive too early can be prevented from triggering the MM by simply gating the transition detector output with a delayed version of the output recovered clock, as shown in Figure 3.7. The outer feedback path pulls the AND gate low until Δ' seconds before the ideal time. The inverter in the feedback path is essential; otherwise the primary pulses will never be able to trigger the MM, since the output of the MM would initially be in the low state. The delay $T_2 = T - T_q - \Delta'$, where T_q is equal to the MM output pulse-width.

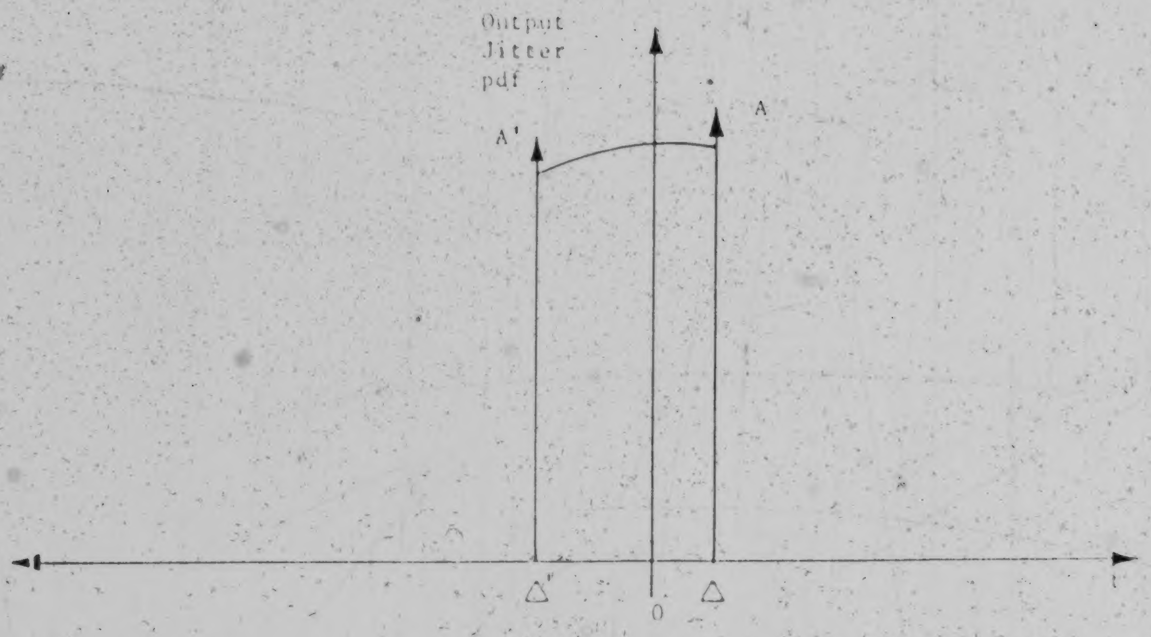


Fig. 3.6 Pdf of the Output Jitter when the Early Primary Pulses are also Inhibited [5]

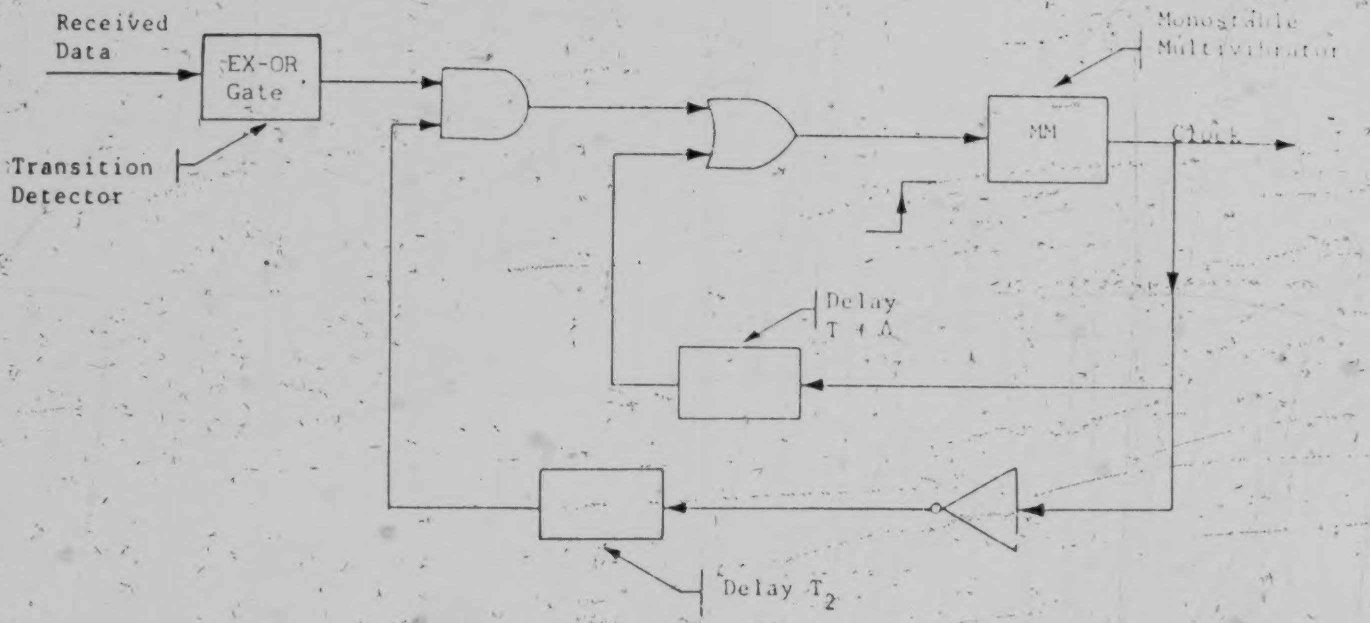

Received Data
EX-OR Gate
Transition Detector
Monostable Multivibrator
MM
Clock
Delay T + Δ
Delay T_2

Fig. 3.7 Modified Monostable Clock Recovery Circuit [5]

3.3.1 A New Version of the Modified MM Clock Recovery Circuit

It was observed during the course of this project that, due to the finite slope and unequal rise times and fall times of the received signal, the pulses generated at the output of the transition detector (EX-OR gate) due to the rising and falling edges of the input signal, were not separated by an integral multiple of the bit interval T. However, pulses due to the rising edges were all at integral multiples of the bit period T; this was true also for the pulses due to the falling edges. A similar problem has been observed by Hill and Butler [75]. They state that, whenever an EX-OR gate is used as phase detector, it gives rise to a positive and negative phase/output voltage characteristic, each having a slightly different gradient due to differences in the EX-OR gate threshold levels. Therefore, to obtain accurate results, it is essential that the same phase characteristic be used for each measurement. This phenomenon was identified only because of the bit-by-bit transition jitter measurements carried out in this project. It could have gone unnoticed if the jitter measurements had been performed by other possible techniques (described in the next chapter). Hence, in order to obtain a clear understanding of the jitter performance of the monostable clock recovery circuit, primary pulses were generated only at the rising edges of the received signal.

The block diagram of the new version of the modified MM clock recovery circuit is shown in Figure 3.8. It only differs from Fig. 3.7 in that the EX-OR gate type of non-linear element is replaced by a monostable multivibrator (MM1) which generates primary pulses only on the rising edge of the received signal. The operation of this circuit can be understood by considering the circuit response to the input bit

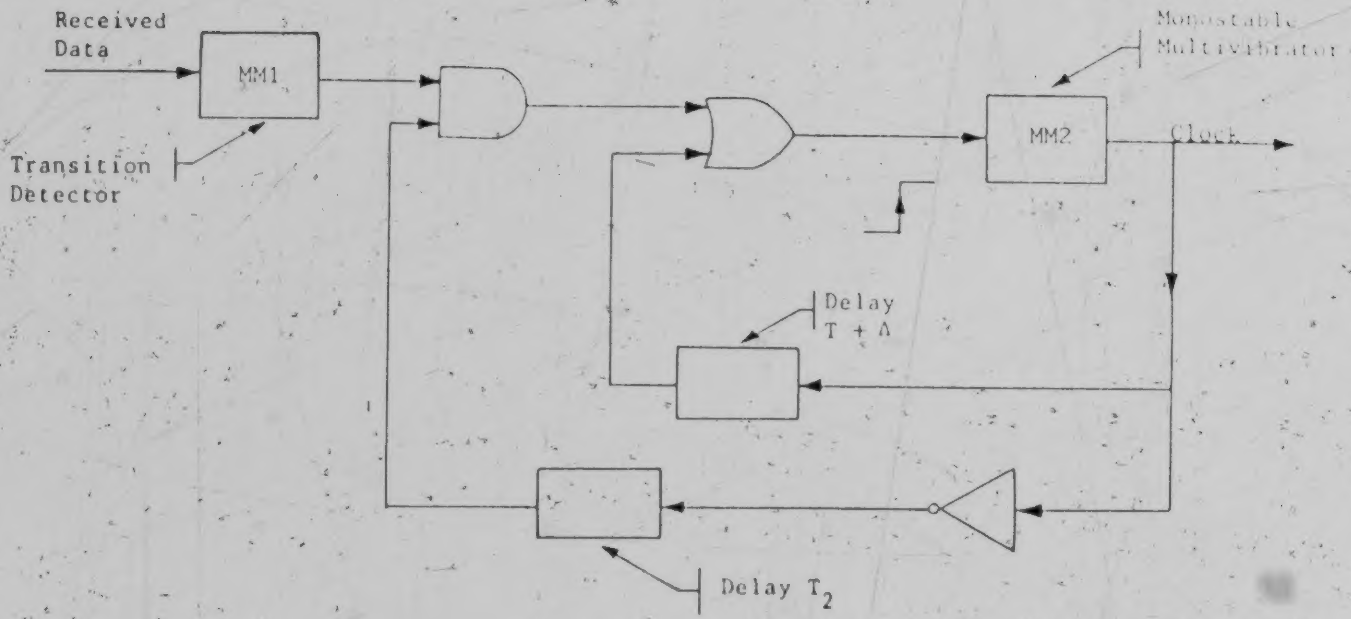

Received
Data
MM1
Transition
Detector
Monostable
Multivibrator
MM2
Clock
Delay
T + Δ
Delay T_2

Fig. 3.8. New Version of the Modified Monostable Clock Recovery Circuit

sequence 10001 (S1), shown in Figure 3.9. The waveform S1 is obtained from the receiver output. The transition detector (MM1) generates a pulse only on every rising edge of the input signal, as shown by S2 in Figure 3.9. The width of these pulses is of sufficient duration to trigger the monostable multivibrator (MM2) of the clock recovery circuit. The monostable multivibrator (MM2) produces a pulse on every rising edge of its input (S4). It can be triggered by the primary pulses of the transition detector, or by the feedback pulses (S5 in Figure 3.9). As can be noted from Figure 3.9, the second, third and fourth bit intervals do not contain a rising edge transition. As a result, the transition detector does not produce a pulse during these intervals (S2). In this situation the feedback pulse triggers the monostable multivibrator (MM2) to produce the clock pulse Δ, 2Δ and 3Δ seconds after the ideal time for the second, third and fourth bit intervals, respectively. In the fifth bit interval, a transition from a 0 to 1 occurs in the input bit sequence and hence a primary pulse triggers the monostable multivibrator (MM2) at the ideal time. Thus, when a long sequence of ones or zeros occur in the input, the clock signal advances in time by Δ seconds during each bit interval until a rising edge transition occurs. This is a simplified description of the new version of the modified MM clock recovery circuit which is valid only when the input jitter is negligible. The remaining details of this circuit are the same as that mentioned in Sections 3.1 and 3.3, respectively.

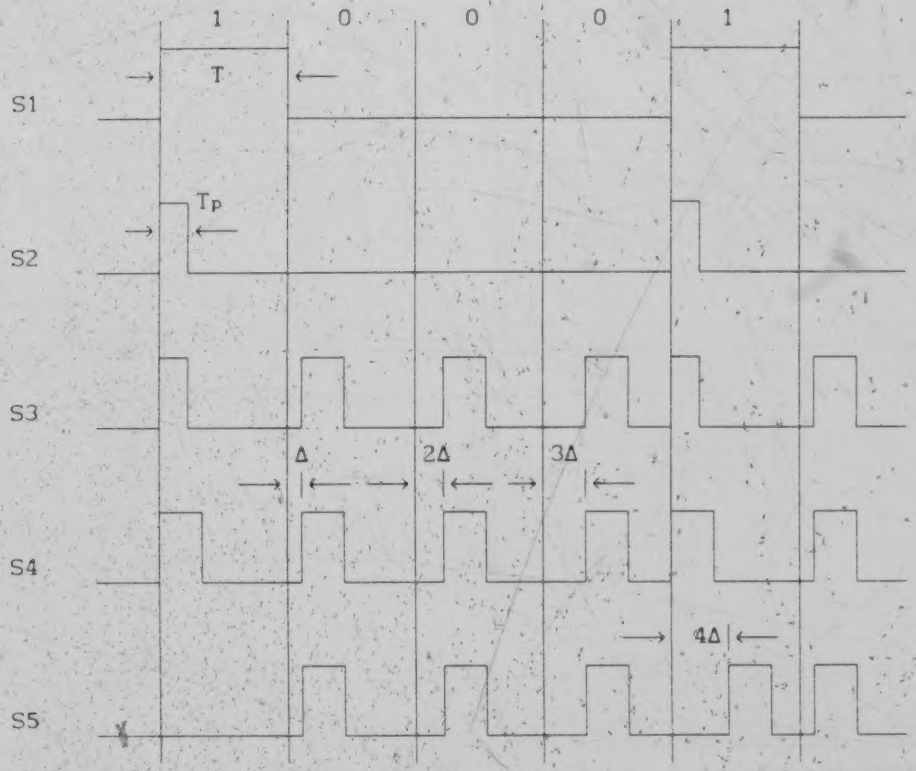

1
0
0
0
1
T
S1
Tp
S2
S3
Δ
2Δ
3Δ
S4
4Δ
S5

Fig. 3.9 Timing Diagram of the New Version of the Self-Sustaining Monostable Clock Recovery Circuit for a 10001 Input Bit Sequence

The next chapter reviews the various jitter measurement techniques and presents the novel jitter measurement scheme implemented in this thesis.

CHAPTER 4

THE MEASUREMENT OF JITTER

Jitter measurement basically involves the detection and measurement of variations in time delay between the significant instants of the digital signal under test with those of the reference signal. The importance of controlling jitter in digital telecommunication systems has been mentioned earlier in this thesis. In order to quantify this important parameter, a number of jitter measurement techniques have been developed. These techniques include approximate estimates of the peak-to-peak jitter, straight-forward phase comparison suitable for commercial applications, and specialized laboratory applications with direct symbol-by-symbol jitter measurement. A brief review of the various jitter measurement methods that have been developed [75-77,81-83] is given first. Later, the technique which was investigated in this project and the method finally adopted are explained.

4.1 Various Methods for Measuring Jitter

4.1.1 Oscilloscope

An estimate of the jitter present on a signal can be obtained by using a high frequency oscilloscope with a very stable linear time base. Using high-speed sampling plug-in modules and adjusting the time axis so that a leading or trailing edge is just within the boundaries of the display, an estimate of the peak-to-peak jitter due to repetitive sources of phase deviation can be read directly from the oscilloscope [75]. This is illustrated in Figure 4.1, where the peak-to-peak jitter is the time interval between the two vertical markers. This scheme gives a relatively good estimate of the jitter

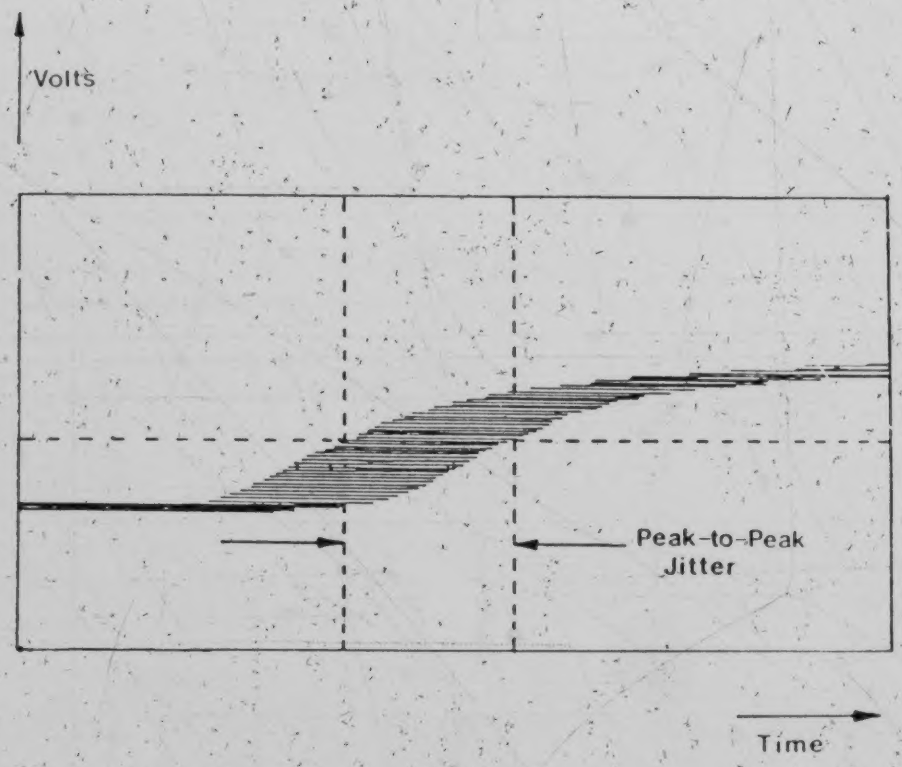

Volts
Peak-to-Peak
Jitter
Time

Fig. 4.1 Oscilloscope Display of Peak-to-Peak Jitter

level, provided that the phase excursions are repetitive in nature or at least, occur frequently. This method is simple but does not allow for an accurate measurement; also, effects due to random jitter will go unnoticed.

4.1.2 Calibrated Baseband Phase Demodulator

As defined earlier, jitter is an unwanted phase modulation present on the received digital signal or on the extracted timing signal. Using a phase demodulator, the received jittered signal may be demodulated and thus converted to a baseband signal that contains the low frequency jitter information. This scheme requires a highly stable phase reference signal which establishes the ideal jitter-free positions in the time domain. The signal under investigation is then compared against the phase reference signal. The calibrated phase demodulator measurement scheme is shown in Figure 4.2.

The two inputs are each passed through a divide-by-two frequency divider, in order to make the phase detector immune to small amplitude differences and wave slopes, and to facilitate jitter measurements whose amplitudes may be several unit intervals (UI) (1 UI= 1 bit period). However, this frequency division reduces the overall accuracy of the measurement.

The "divided down" signals are then applied to an EX-OR phase sensitive detector, whose output contains a stream of pulses whose widths are proportional to the phase difference between the signal under test and the reference signal [76]. A slightly different version of the calibrated phase demodulator produces a stream of pulses at the output of the phase detector whose amplitudes are proportional to the jitter.

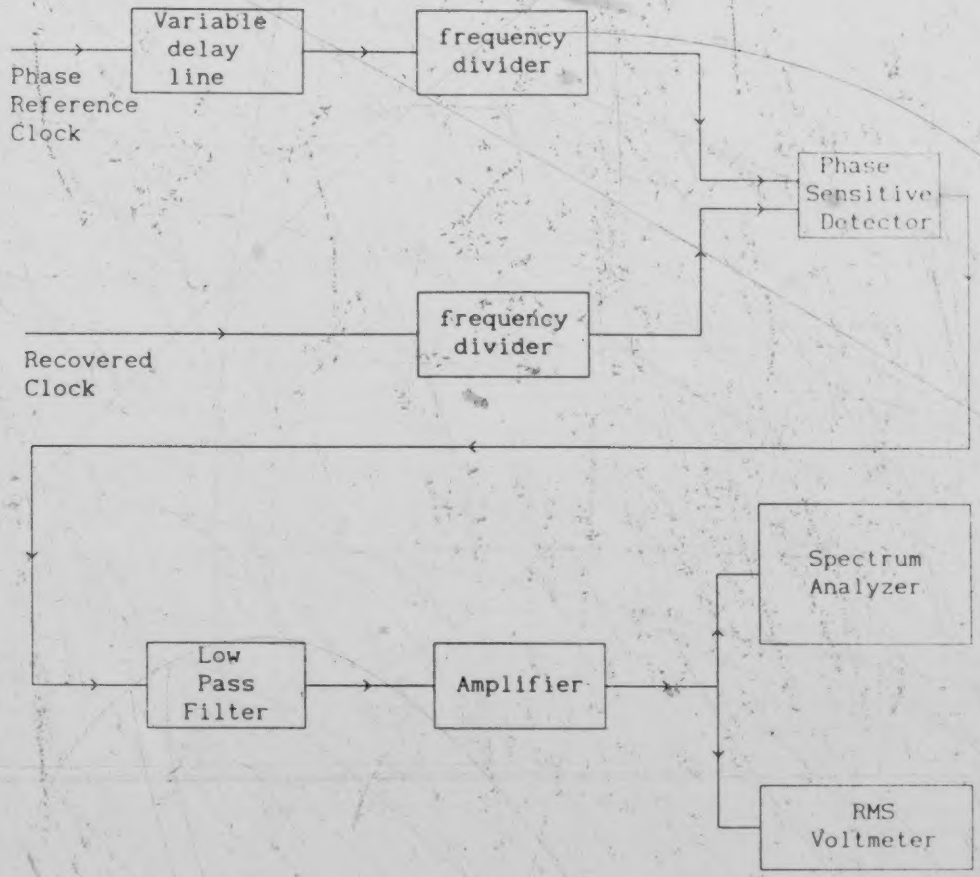

Variable delay line
frequency divider
Phase Reference Clock
Phase Sensitive Detector
frequency divider
Recovered Clock
Spectrum Analyzer
Low Pass Filter
Amplifier
RMS Voltmeter

Fig. 4.2 Schematic of Calibrated Phase Demodulator

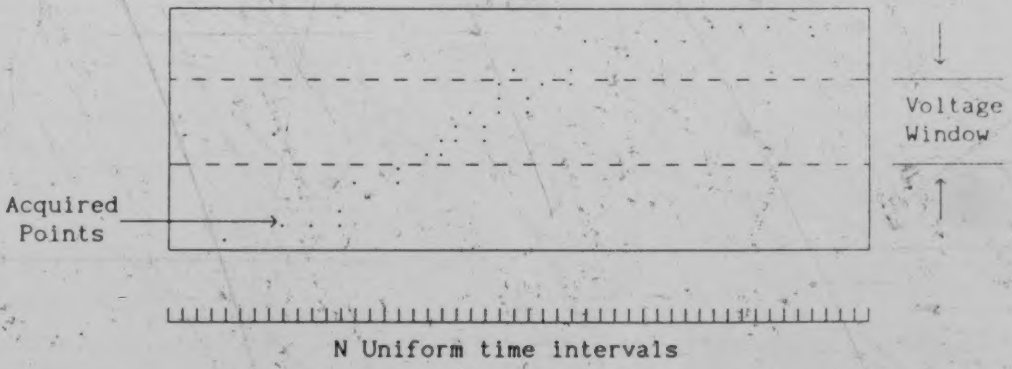

Voltage Window
Acquired Points
N Uniform time intervals

Fig. 4.3 Digital Processing Oscilloscope Display [75]

The output of the phase detector, which contains either a pulse width modulated (PWM) or a pulse amplitude modulated (PAM) stream of pulses, is passed through a low pass filter (LPF) to remove the line frequency component [77]. The LPF output is a continuous analog signal representing the jitter present on the stream of pulses under test. This output is amplified and applied to a RMS voltmeter or to a spectrum analyzer. The voltmeter gives the RMS value of the jitter, defined by σ. The spectrum analyzer gives the power spectral density of the jitter. Ignoring the DC offset, which is due to the static phase shift between the stream of pulses under test and the reference signal, the area under the spectrum is proportional to the jitter power. If we assume that the input jitter is Gaussian, then the jitter power is equal to the jitter variance.

There are certain problems associated with the calibrated baseband phase demodulator [24]. These are:-

a) Sensitivity to amplitude and wave-shape changes at the demodulator input.

b) Poor linearity to small phase deviations if there exists a large static phase shift at its input. This is because the phase demodulator may be driven into its non-linear region. A variable delay line should be used to adjust the static phase shift to 0°.

c) A phase comparator can typically measure a peak-to-peak jitter of upto about 180°. A high amplitude, low-frequency jitter in excess of 180° drives the demodulator into the non-linear region. The phase detector then reads a low value for jitter due to the limiting action of the amplifier and filter following it. Thus the calibrated phase demodulator has poor linearity for wide phase deviations.

d) A balanced phase detector gives rise to both positive and negative phase/output voltage characteristic having different gradients. This is due to the difference in the threshold levels of the EX-OR gate for the rising and the falling edges. As a result, the detector operates for either a 0° or 180° static phase offset between its two inputs. For good repeatability, the same phase characteristic has to be used for each measurement. Thus the calibrated phase demodulator suffers from an imbalance between phase deviations of opposite sign. A similar problem was observed during this project when an EX-OR gate was used as a transition detector as discussed in Section 3.3.1.

Although the calibrated phase demodulator technique has been widely used in the commercial development of jitter measuring instruments [78-80], it is not suitable for a detailed statistical analysis of jitter properties. The main drawback of this method of measuring jitter is that the LPF attenuates the high-frequency jitter components. It disguises the discrete nature of jitter, which is defined only once per symbol at the ideal timing instant. The LPF provides a readily measurable analog signal representative of jitter, but does not allow assignment of precise jitter values on a symbol-by-symbol basis. The study of high-frequency jitter is, however, important for the understanding of the way in which jitter accumulates in long-haul systems [81].

4.1.3 Digital Processing Oscilloscope

A more detailed description of the statistical phenomena of jitter is obtained using a digital processing oscilloscope (DPO) [82,83]. This measurement scheme gives a time and amplitude quantized histogram estimate for the probability density function (pdf) of the transition times of a digital signal. Jitter is measured on the signal directly without any translation of the signal to baseband. This technique is independent of the data rate or format of the signal under test.

The jittered signal is displayed on the DPO using the reference unjittered signal as the trigger. The portion of the jittered signal having the maximum slope is centered on the display of the scope and is made to pass through a voltage window in the minimum time. Hence the exact time at which the signal passed through the window is known, and any spreading which occurs due to the jitter between the two signals at the input is observed. Also, by using high-speed sampling plug-in units, the time axis is extended until the jittered signal is just contained within the boundaries of the display.

The timing instants at which the signal passes through the window can be determined more accurately by decreasing the height of the voltage window and increasing the resolution of the time axis. The time axis is divided into a number of uniform intervals. Points on the waveform are acquired by equivalent time sampling [84]. Each of these acquired points lies in a particular time interval. The sampling process continues until at least a single point is acquired in each time interval. This corresponds to a single scan of the sampling process (Fig. 4.3).

The number of points lying within each interval is then multiplied by an indicator function which is unity for points falling within the voltage window and zero for all other points. Non-zero values for the indicator function denote the time interval during which signal transitions have been detected.

A number of waveforms are acquired and the same operation is performed on each of them. By summing up the number of points falling within each time interval, for every waveform acquired, a histogram estimator for the pdf of jitter is built up. Using the histogram the peak-to-peak jitter can be obtained by measuring the displacement of the extreme points along the time axis. The RMS jitter between the signal under test and the reference signal may also be evaluated.

This method gives a direct estimate of the jitter pdf. On the other hand, it suffers from the same limitations as that of the calibrated phase demodulator. That is, it does not give the high-frequency bit-by-bit jitter on a single-shot basis and hence does not throw light on how jitter accumulates in a regenerator. The measurements rely heavily on the selection of the window width. Choosing a large window size reduces the measurement time but introduces some inaccuracy into the results. If a small window is chosen, a severe measurement time penalty is involved as a number of scans have to be made to obtain a smooth reproducible pdf. In such a case, the equipment has to be stable for the duration of the measurement. Thus, this measurement scheme depends to a great extent on the operator settings.

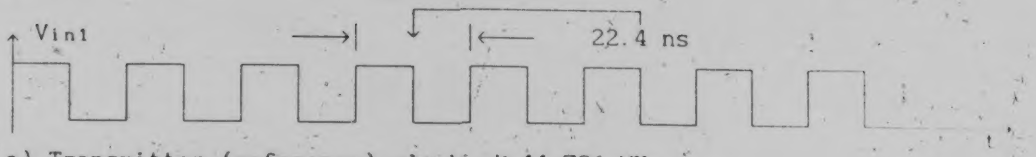
4.1.4 Symbol-by-Symbol Jitter Measurement

This technique measures the jitter present in a digital symbol stream, on a symbol-by-symbol basis. The phase reference signal and the jittered signal under investigation are used to generate two streams of pulses. Both streams of pulses are required to have the same width, height and flatness. The difference between these two derived pulse streams is integrated to generate a stream of pulses whose heights are made proportional to the timing jitter between the two input streams. By measuring the pulse heights, a record of the symbol-by-symbol jitter is obtained. This scheme also has a measurement sensitivity independent of the data rate, being dependent only on the amplitude of the generated pulse streams and on the integrator gain constant [81].

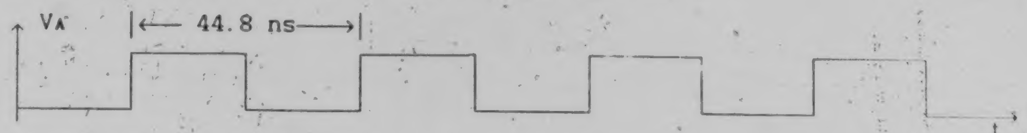
Jitter amplitudes as low as 1 ps can be measured using this scheme provided that the necessary components and equipment are available. The wide bandwidth of the PAM waveform proportional to jitter implies a need for precision in the pulse generation, since any irregularities in pulsewidth, height or flatness appears as noise on the waveform. The design of the integrator presents the greatest challenge for implementation, requiring Op-Amps with a unity-gain bandwidth as large as 1 Ghz.

4.2 PWM to PAM conversion technique

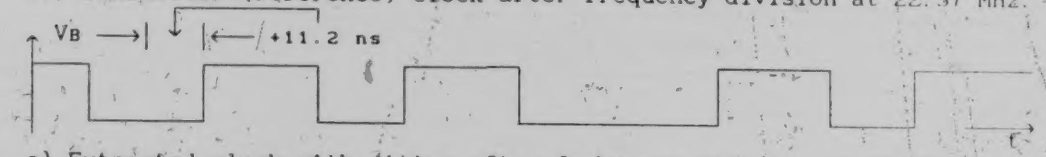
A timing jitter measurement scheme is presented, which allows measurement of the jitter in a digital bit stream on a bit-by-bit basis. The output of the phase detector circuit is a series of rectangular pulses whose widths are proportional to the phase difference between the transmitter clock and the extracted clock. The clock is extracted from the received digital signal using a monostable multivibrator clock recovery circuit. The output of the phase detector can be considered to be pulse width modulated (PWM) by the amplitude of the timing jitter on a bit-by-bit basis. By integrating the widths of the pulses at the output of the phase detector, a stream of pulses is obtained whose heights or amplitudes are proportional to the time delays between the two clocks (Fig.4.4). By measuring the amplitudes of these pulses, a record of the bit-by-bit timing jitter is obtained.


Vin1
22.4 ns
t

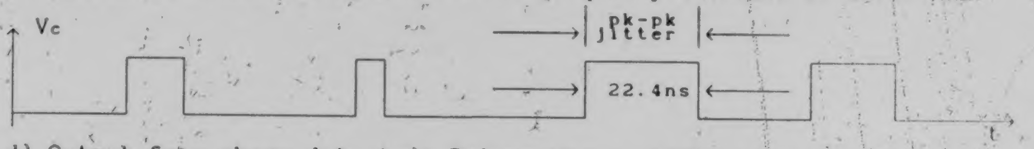
a) Transmitter (reference) clock at 44.736 MHz.



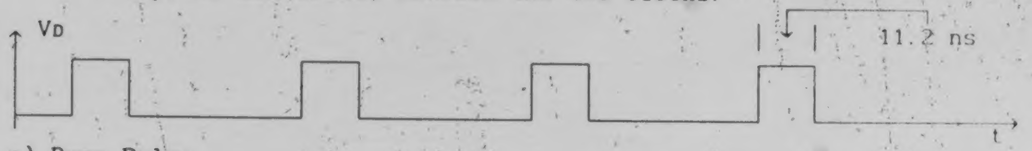
b) Transmitter (reference) clock after frequency division at 22.37 MHz.



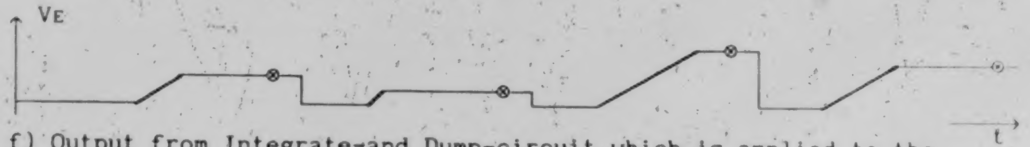
c) Extracted clock with jitter after frequency division at 22.37 MHz.


Vc
pk-pk jitter
22.4ns
t

d) Output from phase detector. Pulses whose widths are proportional to the phase difference between the two clocks.



e) Dump Pulse



f) Output from Integrate-and Dump-circuit which is applied to the digitizing oscilloscope.

⊗ - Samples taken by the digitizing oscilloscope.

Fig. 4.4 Timing diagram of the Jitter Measurement Scheme.

The measurement sensitivity is independent of the data rate. It is dependent only on the amplitude of the reference and extracted clock pulse streams and on the integration time; i.e., on dV/dt. In our jitter measurement system the amplitude of the pulses for worst case jitter is 1 Volt and the peak-to-peak jitter allowed is 22.4 ns (± 11.2 ns). Thus, the measurement sensitivity is 44.6 μV/ps (1V/22.4 ns). Ultimate measurement resolution depends on the vertical resolution of the digitizing oscilloscope and on the noise in the measurement system.

Frequency Divider and Phase Detector Circuit

Figure 4.5 illustrates the block diagram of the jitter measurement system which was initially developed for this project. The circuits were implemented on three different printed circuit (pc) boards. In order to minimize reflections, fifty ohm microstrip transmission lines were used and the interconnections were kept as short as possible. Since high speed operation was desired, MECL 10KH gates were used. Careful circuit layout and strict adherence to a matched-transmission line environment were followed throughout. The signalling is done at the DS-3 rate (44.736 Mb/s). In order to have sufficient time for sampling, and discharging the capacitor in the integrate and dump circuit the clock frequency is divided by two. As a result, a clock waveform of period 44.8 ns is used for the jitter measurement process. The extracted clock signal is also divided by two (Fig. 4.4). Frequency division of the two clock signals is accomplished by using T - flip flops (IC 1 & IC 2) shown in Figure 4.6. Both the clock signals have a duty cycle of 50%. Initially, the extracted clock signal (V_B) which has jitter present on it is adjusted to have a static phase offset of 11.2 ns (+ 90°) with respect to the

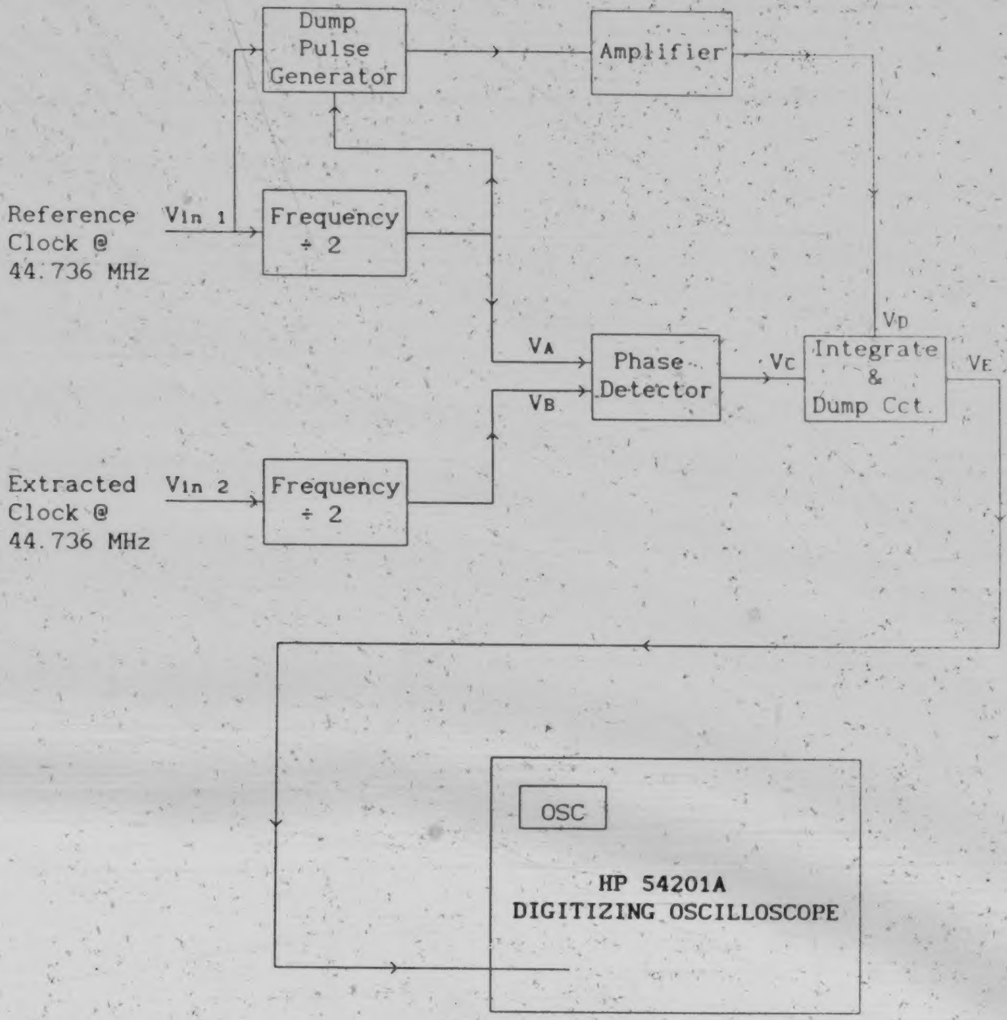

Dump Pulse Generator
Amplifier
Reference Clock @ 44.736 MHz
Vin 1
Frequency ÷ 2
VD
VA
Phase Detector
VC
Integrate & Dump Cct
VE
VB
Extracted Clock @ 44.736 MHz
Vin 2
Frequency ÷ 2
OSC
HP 54201A DIGITIZING OSCILLOSCOPE

Fig. 4.5 Experimental Jitter Measurement System

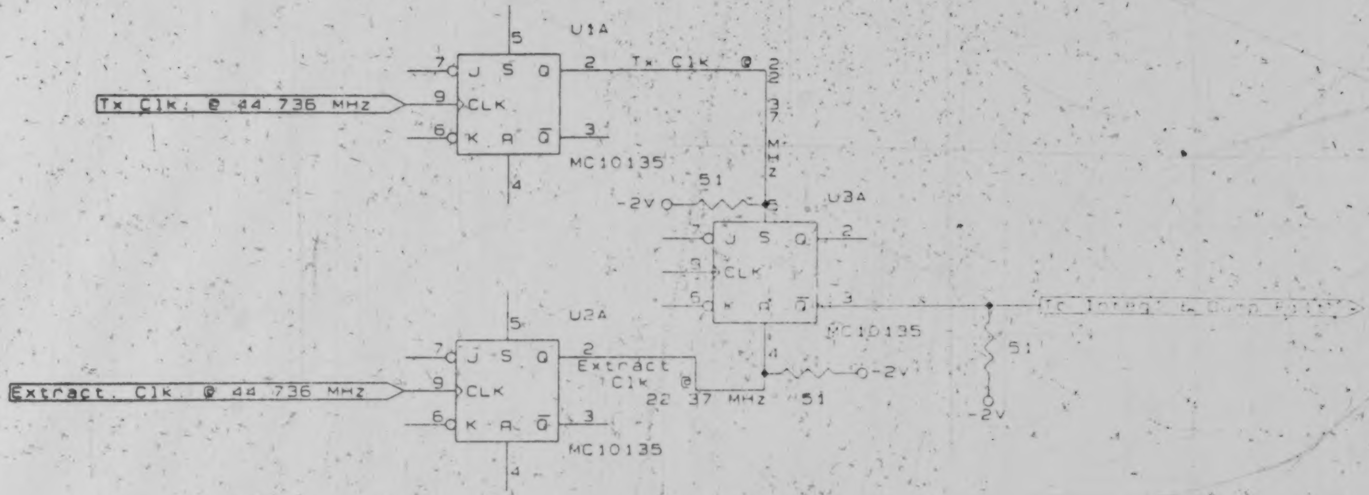

Tx Clk @ 44.736 MHz
Extract. Clk. @ 44.736 MHz
U1A
U2A
U3A
MC10135
MC10135
MC10135
J
S
Q
CLK
K
R
Q̄
5
7
9
6
2
3
4
Tx Clk @ 22.37 MHz
Extract Clk @ 22.37 MHz
51
51
51
-2V
-2V
-2V
To Integ. & Dump Filter

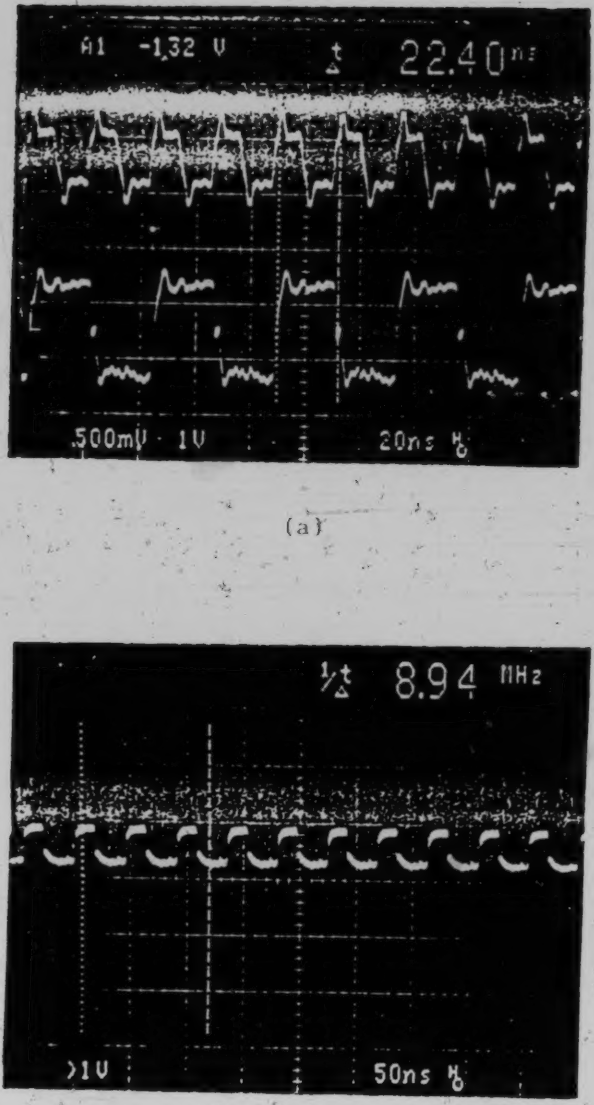
Fig.4.6 Frequency Divider and Phase Detector Circuit

phase reference clock (V_A). With such an arrangement the recovered clock could either arrive 11.2 ns earlier or 11.2 ns later than the ideal reference clock. In other words, the peak-to-peak jitter allowed is 22.4 ns (± 11.2 ns). The phase detector is an R-S flip flop (IC 3) which triggers only on the rising edge. The rising edge of the reference or transmitter clock sets the flip-flop and the rising edge of recovered or extracted clock resets the flip-flop. Thus the output of the phase detector is a stream of pulses whose widths are proportional to the timing jitter. As the peak-to-peak jitter allowed is ± 11.2 ns, the output of the phase detector is a stream of pulses whose widths lie between 0 to a maximum of 22.4 ns (worst case jitter). Hence, the maximum integration time is 22.4 ns. Out of the remaining 22.4 ns available before the beginning of the next cycle, 11.2 ns each is alloted for sampling and dumping. Since high speed operation is desired, emitter coupled logic (ECL 10KH family) gates were used. These have a propagation delay of 1 ns and typical transition times of 1.8 ns. Figures 4.7 (a) and (b) show the waveforms at the output of the frequency divider and phase detector.

Integrate-and-Dump Filter

The integrate-and-dump filter is required to convert the pulse width proportional to jitter (output from the phase detector), to pulse amplitude. The basic requirement of this filter is that the output voltage be linearly proportional to the width of the pulse.

The integration cycle is accomplished by using a BJT differential-pair configuration, as shown in Figure 4.8. It consists of two matched transistors, Q_3 and Q_4, whose emitters are joined together and biased by a transistor (Q_2) constant-current source. A



Reference Clock @ 44.736 MHz.

Reference Clock @ 22.37 MHz.

(a)

Phase difference of 20 ns between the two clocks.

(b)

Fig. 4.7 Waveforms at the Output of the
(a) Frequency Divider of the Reference Clock
(b) Phase Detector

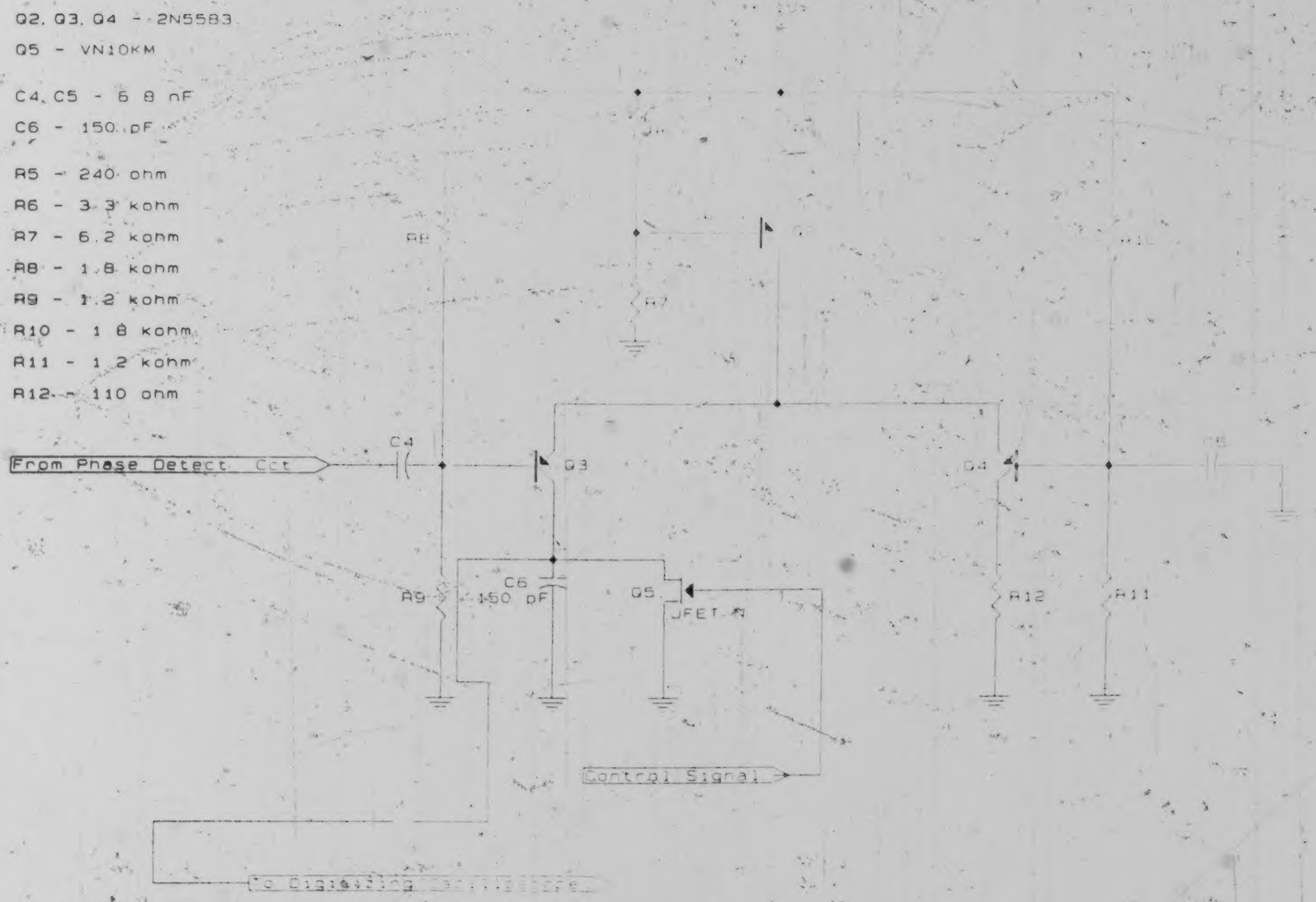

Q2, Q3, Q4 - 2N5583
Q5 - VN10KM
C4, C5 - 6.8 nF
C6 - 150 pF
R5 - 240 ohm
R6 - 3.3 kohm
R7 - 6.2 kohm
R8 - 1.8 kohm
R9 - 1.2 kohm
R10 - 1.8 kohm
R11 - 1.2 kohm
R12 - 110 ohm
From Phase Detect Cct
C4
R8
R7
Q3
Q4
C5
C6
150 pF
R9
Q5
JFET-N
R12
R11
Control Signal
To Digitizing Oscilloscope

Fig. 4.8 Integrate-and-Dump Filter

capacitor (C_6) at the collector of Q_3 is charged for a length of time that is equal to the width of the pulse from the phase detector. The transistors Q_2, Q_3 and Q_4 are all DC biased such that they remain in the active region for the amplitude range of the input signal. The base of Q_4 is AC grounded. With the configuration of Fig. 4.8, Q_3 conducts only when the signal at its input goes negative. Thus the inverted version of the phase detector output (proportional to jitter) is applied to the input of the differential amplifier. Since

$$Q = C\ V$$
$$I = dQ/dt = C\ dV/dt. \qquad \ldots(4.1)$$

The phase detector output has an amplitude of 1 V (dV) and the maximum pulse width is 22.4 ns (dt). Choosing a capacitance of 150 pF for C_6, the required bias current I is equal to 6.7 mA. When the input signal (V_c) to the differential amplifier is in the low state, the transistor Q_3 is switched on and the entire bias current I flows through the collector of Q_3 to charge the capacitor C_6. The capacitor is charged for the duration of time that the input signal is in the low state. When V_c changes state, the transistor Q_3 switches off and the integration cycle is completed.

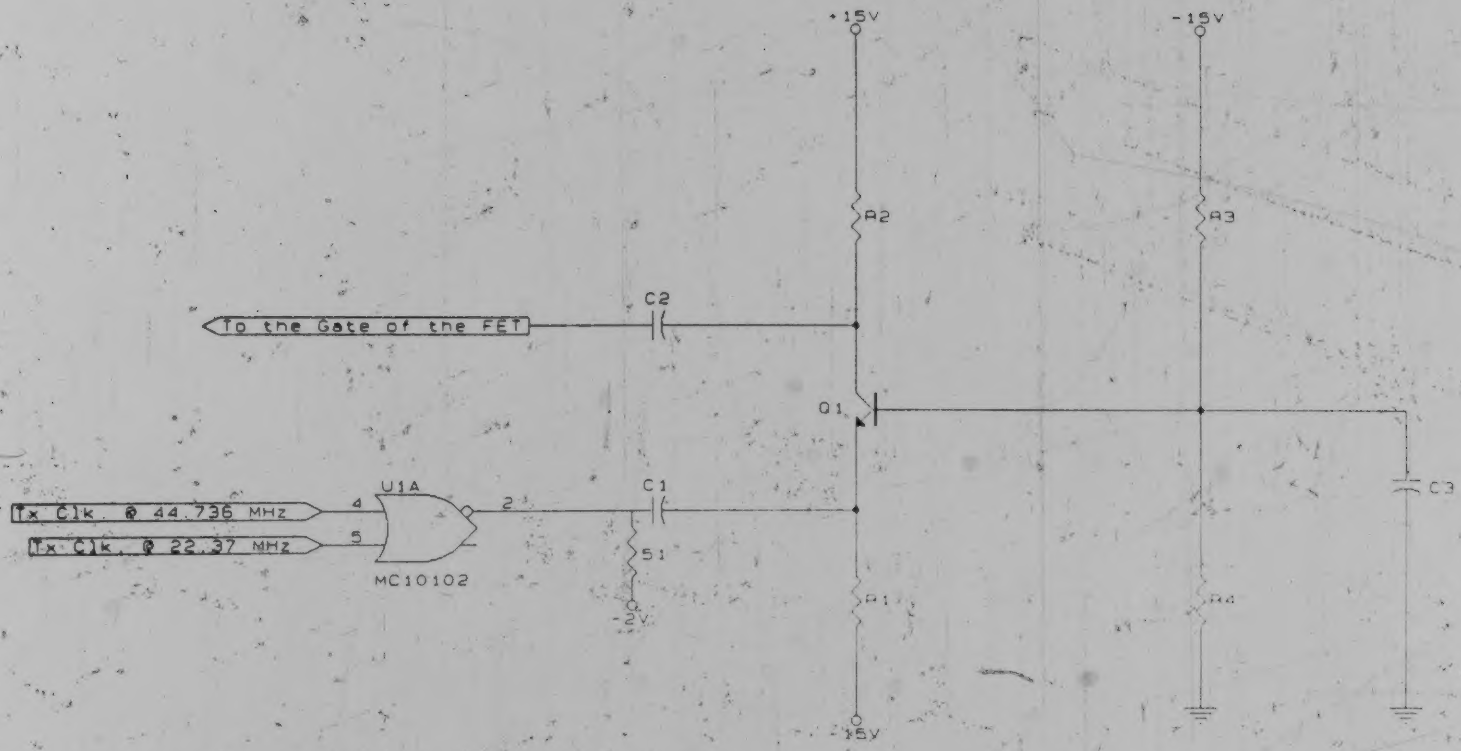
A VMOSFET (VN10KM) across the capacitor (C_6) is used to discharge the capacitor (dump cycle). In order to provide a short period of time during which the peak output voltage may be sampled by the digitizing oscilloscope, the FET (Q_5 of Fig. 4.8) is arranged to turn on approximately 11.2 ns after the integration period. The FET is used as an analog switch. Whenever the gate signal V_D (amplified dump pulse) is above the pinch-off voltage of the FET (in this case 2.0 V), the FET is turned on such that the drain-source resistance (r_{ds}) is very small (approx. 5 ohms). Then, the charged capacitor (C_6) discharges through the FET and the voltage across it becomes equal to zero.

Dump Pulse Generator and Amplifier

The schematic diagram of the dump pulse generator and amplifier is illustrated in Figure 4.9. The dump pulse serves as the control signal to turn the FET on and off in order to charge and discharge the capacitor. The dump pulse is generated by a NOR gate. Signals V_{ini} and V_A (Fig. 4.4) are applied to the NOR gate. A dump pulse of width 11.2 ns, which is equal to the time the two input signals are in the low state, is generated. The pulse also occurs 11.2 ns after the integration cycle is completed, to allow for sampling the peak voltage across the capacitor (C_6).

Since the pinch-off voltage of the FET is approximately 2 volts, a signal of amplitude larger than 2 volts is required to turn the FET on. As the output from the ECL NOR gate has an amplitude of only 1 volt, it needs to be amplified further before it can serve as the control signal to the gate of the FET. This amplification is carried out by the common base amplifier shown in Figure 4.9. The amplified dump pulse (V_D) is then used to control the FET. The gain of the common base amplifier was around 3. A high frequency Motorola npn transistor BFR 91, having an f_T of 5 GHz, was used. Figures 4.10 (a), (b) and (c) show the waveforms at the input of the common base amplifier, the amplified output which is applied to the gate of the FET and the signal at the drain of the FET, respectively.

Figure 4.11 shows the waveform at the output of the integrate-and-dump circuit. As can be seen from this figure, for an input square wave of period 44.8 ns, the capacitor charges for 22.4 ns,


+15V
-15V
R2
R3
C2
To the Gate of the FET
Q1
C3
U1A
Tx Clk. @ 44.736 MHz
Tx Clk. @ 22.37 MHz
4
5
2
C1
51
MC10102
-2V
R1
R4
15V

Q1 - BFR 91

C1, C2, C3 - 6.8 nF

R1 - 2.2 kohm
R2 - 4.3 kohm
R3 - 2.2 kohm
R4 - 1.1 kohm

Fig. 4.9 Dump Pulse Generator and Amplifier

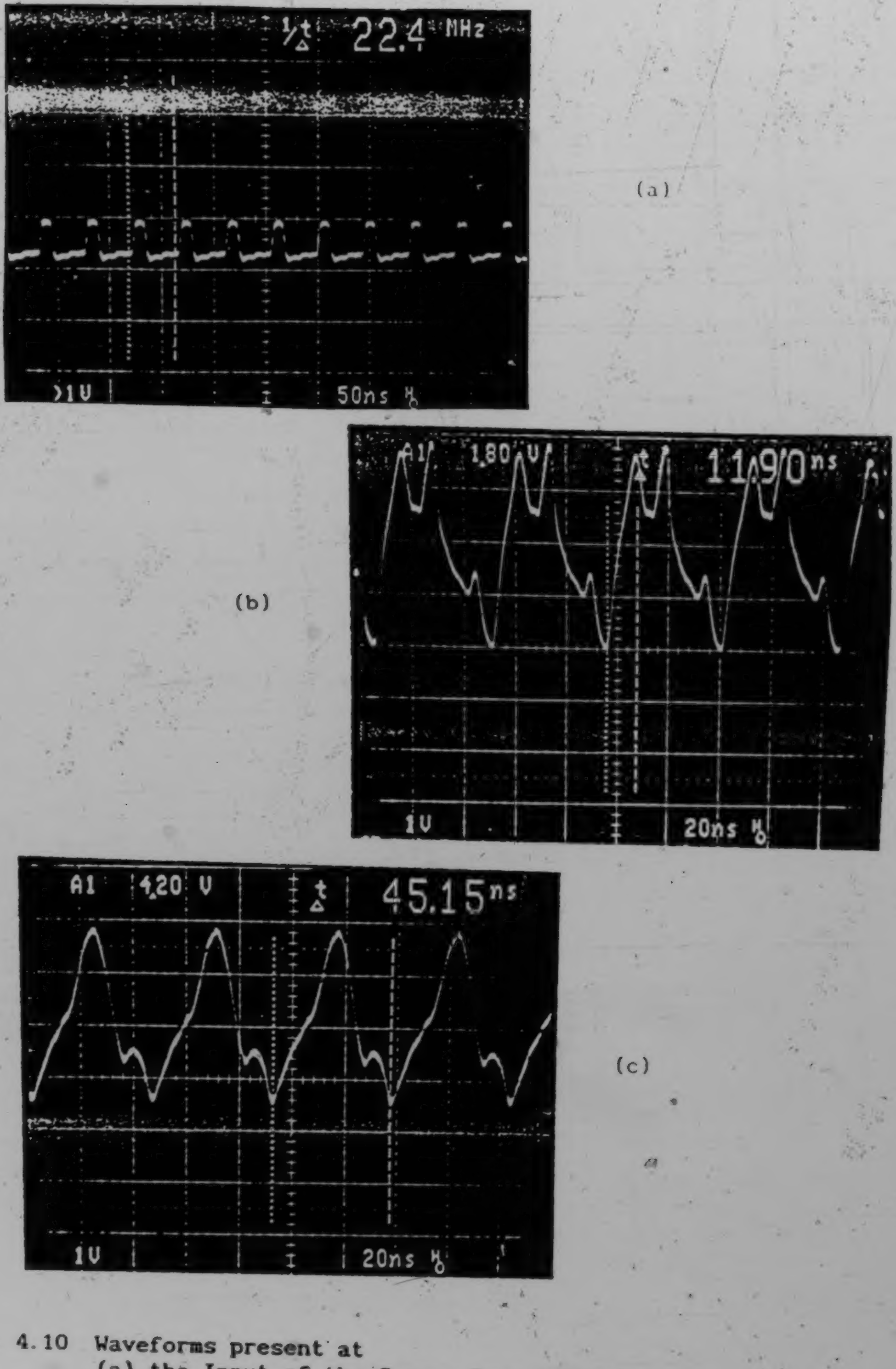
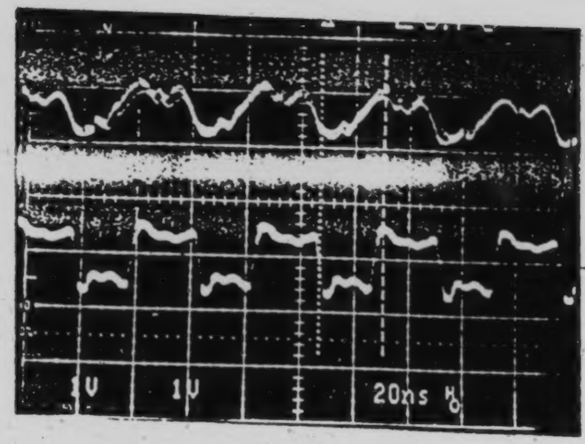


Fig. 4.10 Waveforms present at
(a) the Input of the Common Base Amplifier.
(b) the Output of the Amplifier, applied to the Gate of the FET.
(c) the Drain of the FET.



Input, Square Wave of 22.37 MHz

Fig. 4.11 Output of the Integrate & Dump Filter at 22.37 MHz.

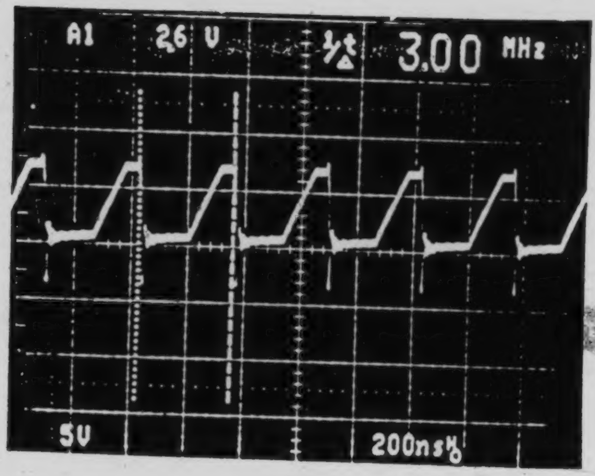


Fig. 4.12 Output of the Integrate & Dump Filter at 3.00 MHz.

then holds and dumps the voltage in the remaining time of 22.4 ns.

In principle, the measurement scheme described in this section is perfectly good. However, the practical performance of this jitter measurement system was not satisfactory at the signalling speed of 22.37 MHz. As it is apparent from Fig.4.11, the charging of the capacitor is not linear with respect to the integration time. This might be due to the fact that, in Fig. 4.10 (a), the width of the input pulse is 11.2 ns and the period is 14.8 ns. After amplification the duration of the pulse increases to 45.15 ns (Fig. 4.10 (b)). Because of this the conduction cycle of the FET is greater than 20 ns (Fig. 4.10 (c)), whereas ideally the time allowed for the discharge of the capacitor is only 11.2 ns. This necessitates a better design for the common base amplifier and the use of a FET having a higher switching speed. Secondly, the noise present at the gate was capacitively coupled to the drain and hence to the charging capacitor. As a result, the output of the integrate-and-dump circuit shown in Fig.4.11 is distorted.

The performance of the same circuit was tested using a square wave at 3.00 MHz. Figure 4.12 shows the output of the integrate-and-dump filter at this rate. It can be seen that the filter performs well at this frequency. The capacitor charges linearly up to a maximum of 7.3V during the time the input signal is in the low state (166.67 ns). It can also be observed from this figure that, there is an undershoot and ringing for a period of about 50 ns before the output settles down to zero volts.

This indicates that the circuit with the components shown can be used up to about 10 MHz. For higher speeds, a better design of the electronic circuit is required using components having a very large bandwidth. Thus, as precise measurements of timing jitter could not be obtained at the signalling rate of 22.37 MHz, this scheme of measurement was abandoned and other methods were explored.

4.3 Jitter Measurement Using a Digitizing Oscilloscope

A new experimental jitter measurement technique was developed to overcome the limitations of the method described in Section 4.2. A measurement method was sought that would eliminate the integrate and dump filter, which was the main limitation of the PWM to PAM conversion technique. The jitter inherent in the recovered clock could be measured by taking advantage of the feature of the high speed digitizing oscilloscope viz., that it can instantaneously sample and store the voltage on a real-time basis. The hardware complexity is reduced to a great extent as no extra circuitry is required. This scheme provides a time and amplitude quantized histogram estimate for the probability density function (pdf) of the transition times of the recovered clock signal. Thus it provides a numerical description of the jitter phenomenon.

In order to acquire a sample at the same point on the waveform during each cycle, the clock frequency must be an integer multiple of the oscilloscope sampling rate of 200 MSamples/s (this was a limitation of the HP54201A oscilloscope). Hence, the signalling rate was changed from the DS-3 rate (44.736 Mb/s) to 50 Mb/s. Thus, the recovered clock has a frequency of 50 MHz (period = 20 ns), a linear rise time of 2.0 ns and an amplitude of 0.7 V. It is applied to Channel 1 of the digitizing oscilloscope. The digitizing scope is made to trigger on the positive crossings of Channel 1. The trigger level is set to 50%

of the peak-to-peak amplitude. The time base is adjusted for a range of 10 μs. At this range the scope has a sampling rate of 100 MS/s (sample period = 10 ns). We assume that the sampling clock of the digitizing oscilloscope is ideal, i.e. it has no inherent jitter, so that it can be used as the reference clock, to determine the timing jitter present on the recovered clock. Once triggered, the scope acquires 1000 samples on a single-shot basis (real-time sampling mode) of the recovered clock. Since the recovered clock waveform has a period of 20 ns and a pulse width of 5 ns, then we obtain for each cycle one sample on the rising edge of the clock pulse and another when the recovered clock pulse is low. (See Figure 4.13). Hence, for each acquisition 500 samples were obtained on the rising edge of the clock waveform, taken at precise intervals of 20.0 nanoseconds.

From these voltage samples, an estimate of the timing jitter on the recovered clock can be determined, using the following argument. In the absence of jitter, the scope acquires a sample at the same point on the waveform (trigger level crossing) during each cycle. However, when the recovered clock pulse arrives later than the ideal time, a sample is taken below the trigger level, while, on the other hand, when the clock pulse arrives earlier than the ideal time, the sample is taken above the trigger level. Using the slope of the rising edge of the clock waveform the voltage differences can be used to determine the time shift, since

$$\Delta t = \frac{s(t_i) - \text{Trigger level}}{ds/dt} = \frac{\Delta V}{\text{Slope of the Signal}} \qquad \ldots(4.2)$$

We have used the convention here that when the recovered clock pulse arrives earlier than the ideal time, then the timing jitter amplitude

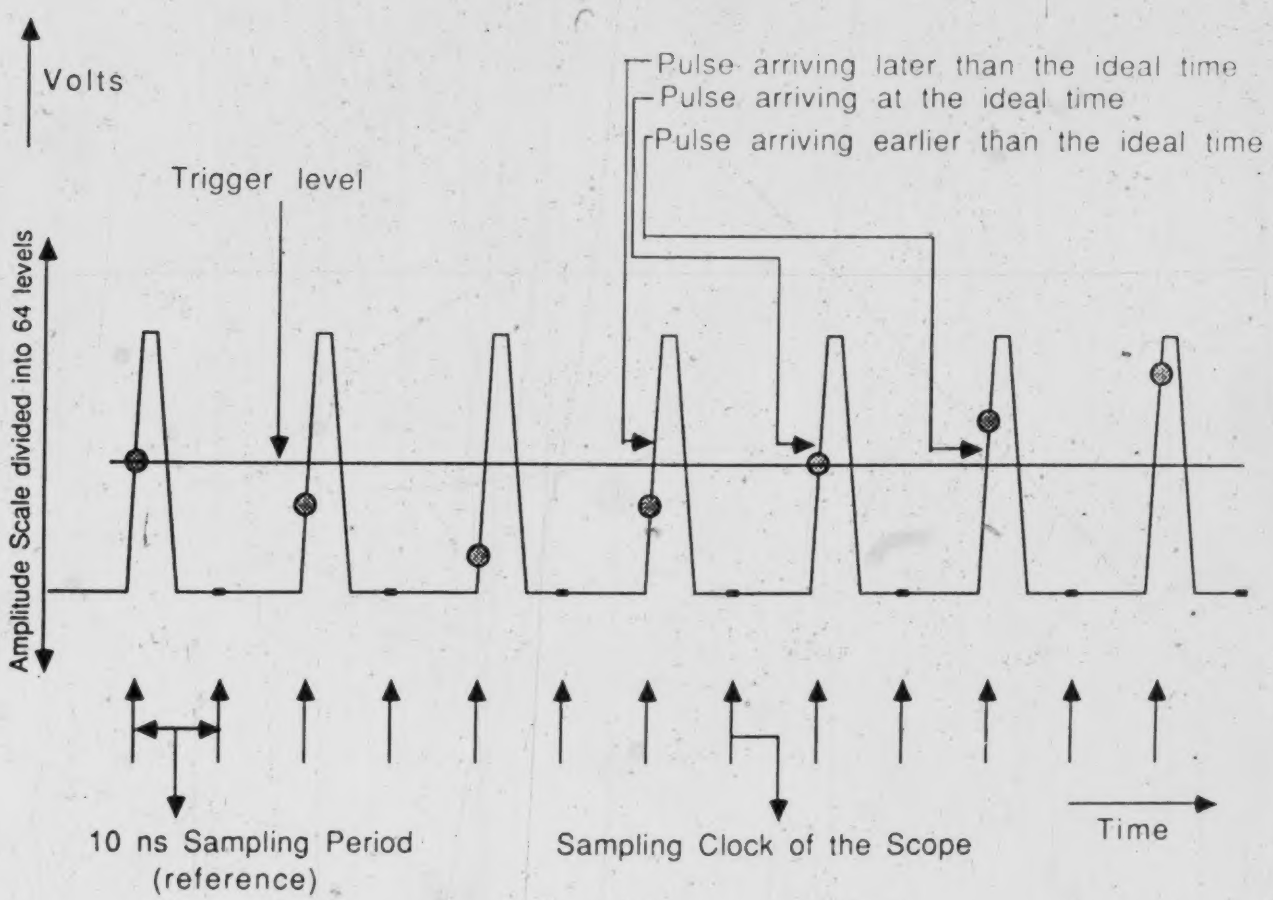

Volts
Trigger level
Amplitude Scale divided into 64 levels
Pulse arriving later than the ideal time
Pulse arriving at the ideal time
Pulse arriving earlier than the ideal time
10 ns Sampling Period
(reference)
Sampling Clock of the Scope
Time

Fig. 4.13 Illustration of the Jitter Measurement Principle.

Δt is positive. The peak-to-peak jitter allowed is only for the time range during which the rising edge is linear, which in our case was 2.0 ns. Thus, the recovered clock pulses could arrive a maximum of 1 ns, earlier or later than the ideal time. This time duration is sufficient to measure the high frequency jitter that may be expected in most practical systems. The trigger level (50% peak-to-peak amplitude) is the mean position around which signal transitions take place.

The amplitude scale (Y-axis) on the display of the digitizing oscilloscope is uniformly partitioned up to a maximum of 64 levels (63 intervals), which we denote as W_1, W_2, ...W_{64}. Subsequent to a single acquisition, a histogram estimate for the probability density function of the voltage differences of the recovered clock is obtained using:

$$p(W_j) = \frac{1}{\Delta W} \cdot \frac{N(W_j)}{\sum_j N(W_j)} ; \qquad j = 1, 2, \ldots\ldots 64 \qquad \ldots(4.3)$$

where $\Delta W = W_{j+1} - W_j$, is the width of each interval on the amplitude scale in volts. $N(W_j)$ is the number of samples $s(t_i)$ which lie on each level W_j $\left(\sum_j N(W_j) = 500\right)$. The mean and variance is then estimated from the histogram data in terms of the amplitude in volts by using:

$$\text{Mean} = \bar{V} = \frac{\sum_j N(W_j) \cdot W_j}{\sum_j N(W_j)} \qquad \ldots(4.4)$$

$$\text{Variance} = \sigma_v^2 = \frac{\sum_j \left[N(W_j).W_j^2 \right] - \dfrac{\left\{ \sum_j \left[N(W_j).W_j \right] \right\}^2}{\sum_j N(W_j)}}{\sum_j N(W_j) - 1} \qquad \ldots(4.5)$$

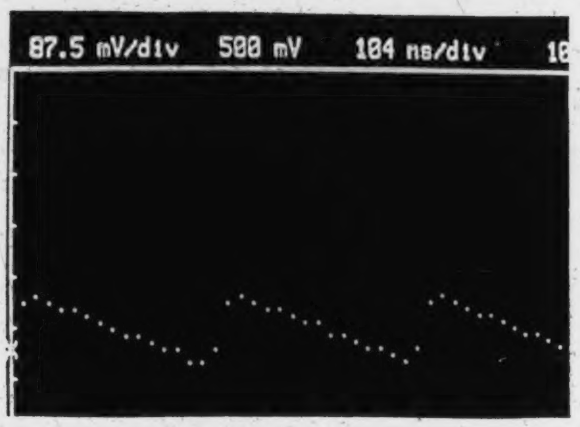
By performing further acquisitions we obtain histograms with distributed means and variances σv_i^2. The Standard Deviation (σ_t) or the mean R.M.S. jitter value may then be found using:

$$\sigma_t = \frac{\sqrt{\text{Mean of the Variances}}}{\text{Slope of the signal}} \qquad \ldots(4.6a)$$

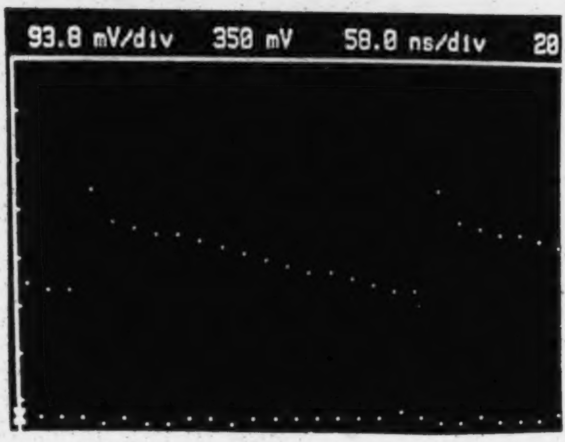
$$\sigma_t = \frac{\sqrt{\dfrac{1}{N} \sum_{i=1}^{N} \sigma v_i^2}}{\text{Slope of the signal}} \qquad \ldots(4.6b)$$

where i = 1, ...N is the number of histograms obtained.

In order to test this measurement principle, an NRZ input data pattern of 1000000000000000 at 50 Mb/s was applied to the original Monostable Multivibrator (MM) clock recovery circuit (EX-OR gate as the transition detector). It is a 16-bit repetitive fixed word pattern. The digitizing scope was set for the conditions mentioned at the beginning of this section. Figure 4.14(a) illustrates the pattern of occurrence of the recovered clock pulses. Each dot represents a sample acquired by the scope on the rising edge of the recovered clock pulse stream. The two dots on the rising voltage level represent the clock pulses at the output of the clock recovery circuit when the MM is triggered by the primary pulses from the transition detector. The transition detector generates only 2 primary pulses for each 16-bit



(a)



(b)

Fig. 4.14 Pattern of Occurrence of the Recovered Clock Pulse Stream
(a) when transition detector generates pulses on both, the rising and falling edges.
(b) when transition detector generates pulses only on the rising edge.

fixed word pattern, one on the rising edge and the other on the falling edge of the "1" bit (refer section 3.1). The remaining 14 dots on the decreasing voltage level stream represent the clock pulses when the MM is triggered by the feedback pulses. Each pulse on the downhill occurs Δ seconds after the previous pulse until a transition from a 0 to 1 occurs.

rom Figure 4.14(a) it can also be observed that the two samples on the rising voltage level do not occur at the same amplitude level. Ideally, they should be at the same level, because these clock pulses should occur at integral multiples of the bit period T (=20 ns) of the input data. The reason for this non-ideal behaviour has been discussed in Sections 3.3.1 and 4.1.2.

In order to eliminate this undesirable effect the clock recovery circuit was modified by re-designing the transition detector. The EX-OR gate was replaced by a Monostable Multivibrator, which generates pulses only on the rising edge of the input data signal. In this thesis, this is referred to as the "new version of the modified MM clock recovery circuit" (Section 3.3.1). The same input data pattern of 1000000000000000 was applied to the modified clock recovery circuit. Figure 4.14(b) illustrates the voltage samples obtained from the recovered clock pulse stream. It can be observed from the figure that for this new clock recovery circuit, the primary pulses from the transition detector, give rise to samples that occur at the same amplitude level, or in other words at integral multiples of the bit period T. Following the "1" bit, we have 15 pulses of decreasing voltage level, as the clock recovery circuit is triggered by the feedback pulses.

The construction of the histogram estimate for the pdf of the transition times and the numerical evaluation of the jitter variance, etc. will be presented in Chapter 6. The next chapter discusses the experimental fiber optic system which was set up, and the measurements which were performed.

CHAPTER 5

THE EXPERIMENTAL FIBER OPTIC SYSTEM

An experimental optical fiber communication system employing the nonreturn-to-zero (NRZ) code was designed and constructed. The main objectives for setting up this experimental system were the following:

1. To investigate the performance of the self-sustaining monostable multivibrator clock recovery circuit when used with the NRZ code.

2. To measure the absolute jitter present on the recovered clock on a symbol-by-symbol basis.

3. To obtain a graphical representation of the probability density function of jitter which would enable detailed jitter statistics to be derived, facilitate the identification of any deterministic structure to the jitter and serve as a valuable diagnostic tool in the investigation of random and data-dependent systematic jitter effects.

A block diagram of the experimental fiber optic system is shown in Figure 5.1. The experimental system consists of a data generator, laser transmitter, multimode optical fiber, avalanche photodiode detector (APD) preamplifier, main amplifier and a clock recovery circuit. The data generator generates binary NRZ data at 50 Mb/s when clocked externally by a 50 MHz sinusoidal, synthesized signal source. The data generator is capable of generating 10 or 16 bit repetitive fixed word patterns with any number of 1s or 0s and also pseudo-random binary sequences (PRBS) of length $2^{10}-1$, $2^{15}-1$ and $2^{23}-1$ bits. This data stream then modulates the laser transmitter. The optical signal from the laser diode, which operates at a wavelength of 0.83 μm, is fed to a multimode optical fiber. At the receiving end, the weak and noisy optical signal is converted to an electrical signal by an APD detector.

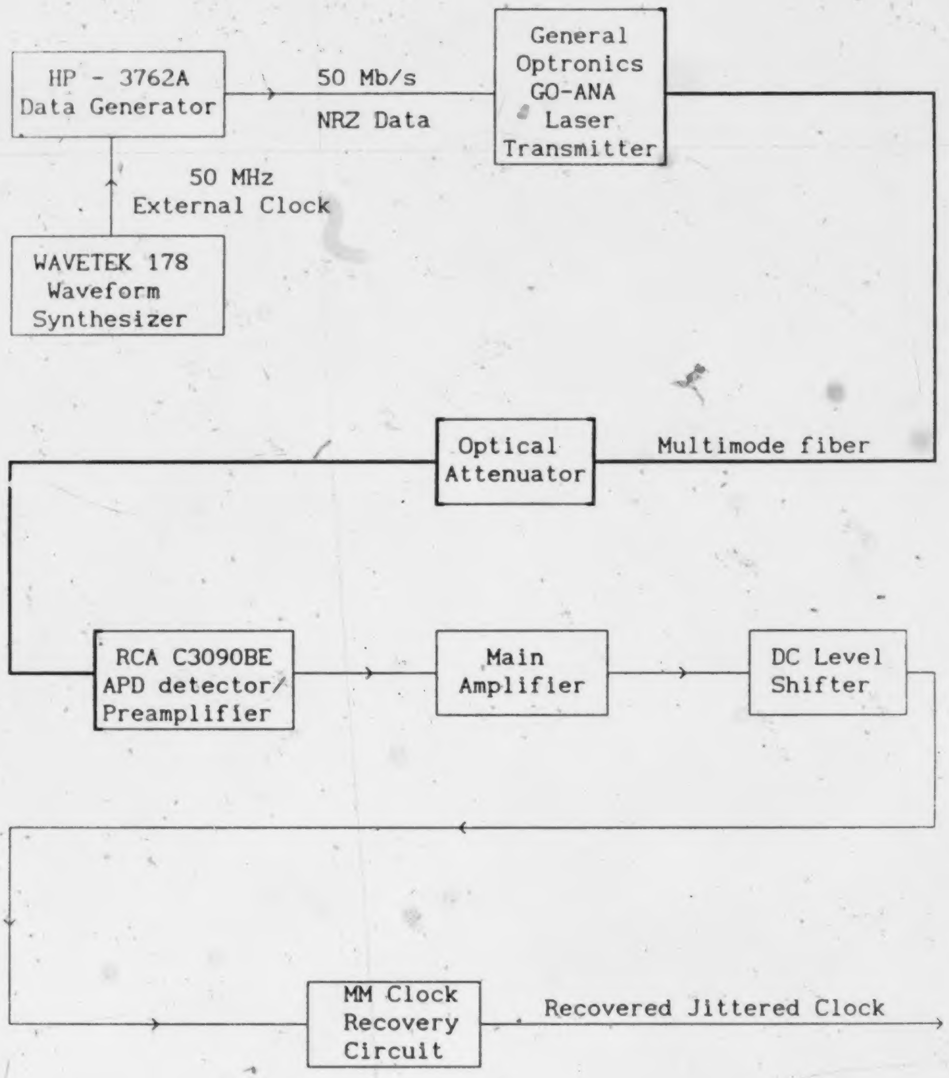

HP - 3762A
Data Generator
50 Mb/s
NRZ Data
General
Optronics
GO-ANA
Laser
Transmitter
50 MHz
External Clock
WAVETEK 178
Waveform
Synthesizer
Optical
Attenuator
Multimode fiber
RCA C3090BE
APD detector/
Preamplifier
Main
Amplifier
DC Level
Shifter
MM Clock
Recovery
Circuit
Recovered Jittered Clock

Fig. 5.1 Block Diagram of the Experimental Optical Fiber System

The signal current produced by the APD is amplified to a useful level with a low noise preamplifier followed by a main amplifier. The output of the main amplifier is, ideally, the original binary NRZ data which was transmitted. The sampling clock required in the decision circuity of the decoder is derived from the received signal by the new self-sustaining monostable clock recovery circuit. In this chapter, the design and operation of each of the experimental components is described in detail.

5.1 Laser Transmitter

A General Optronics short wavelength 830 nm single longitudinal mode laser diode was used for the optical source. This laser diode has the drive circuitry, which incorporates automatic power and temperature control and performance warning alarm, built into the same package (model GO-ANA). The laser can be modulated over a frequency range of 20 Hz to 1.25 GHz, has an average coupled output power of 1 mW, and has a fairly linear output power versus current characteristic. The electrical input to the laser transmitter is capacitively coupled and has an impedance of approximately 50 ohms. The laser is biased at the centre of its linear operating region. An input peak-to-peak voltage swing of 0.8 volts is sufficient to turn off the laser for the zero level.

5.2 Optical Fiber

The experimental fiber optic system utilizes graded index, multimode fiber manufactured by Northern Telecom. This fiber has a numerical aperture of 0.2, an average attenuation of 2.75 dB/km, and a dispersion of 1.5 ns/nm-km (FWHM) at a wavelength of 0.83 μm. The experimental system was tested with 5 km. of fiber. A variable optical attenuator with the matching fiber optic connectors was not available in the laboratory. In order to control the amount of optical power incident on the APD detector, a short length of fiber was wound around a glass rod of approximately 1 cm. in diameter. In this way, power loss was achieved by microbending of the optical fiber [85].

Multimode optical fiber was used in this project because it was readily available in the laboratory, together with the proper connectors for the laser source and the APD receiver. Single mode fiber and a long wavelength source at 1300 nm or 1500 nm could also be used, in which case, a considerably longer length of fiber would have been required because of the lower dispersion of the single mode fiber and the lower fiber attenuation at longer wavelengths. However, since a sufficient length of single mode fiber with proper connectors was not available in the laboratory it could not be used.

The 3 dB electrical bandwidth of the fiber (F_{3dB}) can be easily determined from the well-known equation [86]:

$$F_{3\,dB} = 311/D \quad \text{MHz.km} \qquad \ldots\ldots(5.1)$$

where D = Pulse dispersion in ns/km (at FWHM)

Since the source has a spectral width of 0.84 nm, the pulse dispersion $D = 1.5$ ns/nm-km . 0.84 nm

$= 1.26$ ns/km

The 3 dB electrical bandwidth from equation (5.1) is then,

$$F_{3\,dB} = 311/1.26 \quad \text{MHz.km}$$

$$= 246.83 \quad \text{MHz.km}$$

Since 5 km of optical fiber was used, the bandwidth for the total section is approximately 246.83 / 5 = 49.37 MHz. This is only a rough estimate; the actual bandwidth may be greater, because the dispersion should be smaller due to mode mixing, which is caused by microbending and splices [86].

The bandwidth of the fiber should be sufficiently large or else a power penalty is incurred at the receiver. According to Senior [87], the maximum bit rate that can be used, without any SNR penalty at the receiver is given approximately by

$$B_T\,(\mathrm{max}) \cong 0.2 / \sigma \text{ bit s}^{-1} \qquad .....(5.2)$$

where σ = 0.5 x RMS pulse width of impulse response of the fiber

= 2.355 D

= 2.97 ns for the experimental fiber.

Therefore, $0.2/\sigma$ = 67 Mb/s. Thus, the bandwidth of the fiber should be sufficient to transmit an NRZ data stream at 50 Mb/s.

5.3 Optical Pre-amplifier

The optical receiver consists of a detector, preamplifier, and main amplifier. The optical detector/preamplifier unit used in this thesis was originally designed and developed by Kumar S. Visvanatha [5]. The sensitivity of the receiver is determined mainly by the noise sources in the preamplifier stage. In order to achieve a low BER, it is necessary to minimize the noise contributions from the optical detector and the front-end electronics, while maintaining the signal integrity. Thus, a proper design of the preamplifier stage is essential for good system performance.

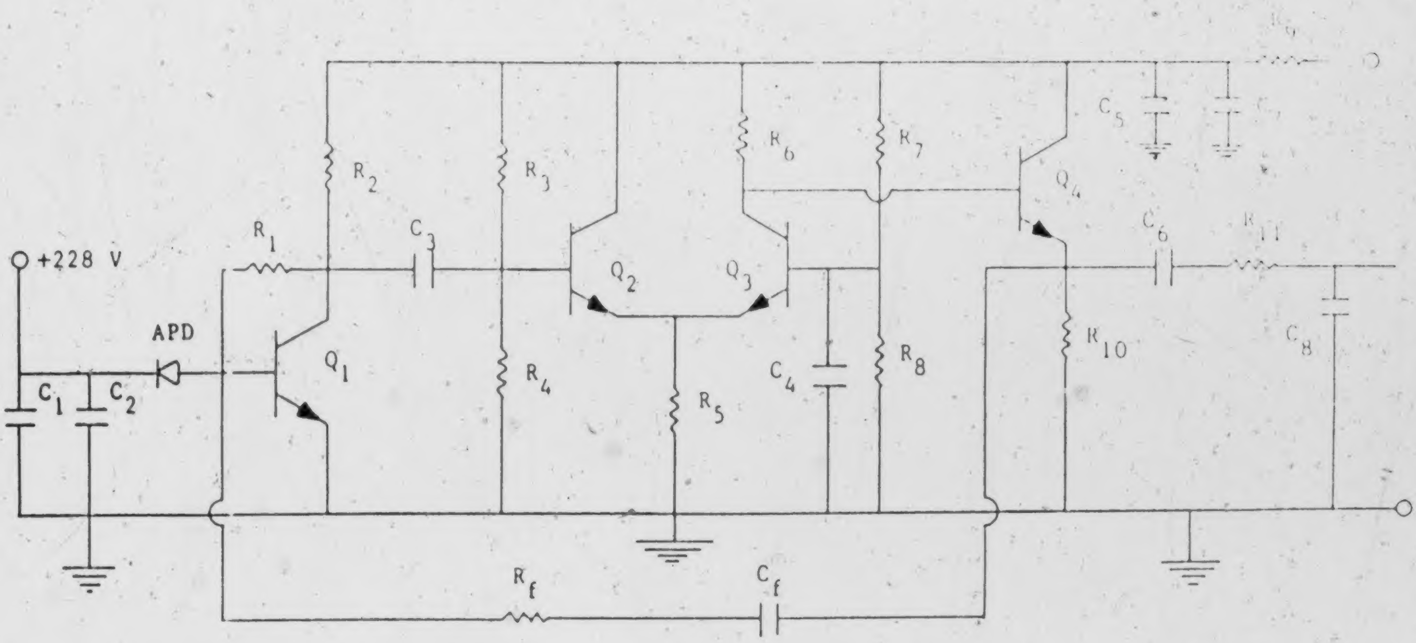
The experimental optical receiver employs a silicon APD followed by a low gain bipolar transimpedance preamplifier. The detector used is an RCA C30908E APD. The main features of this APD are as follows: operating voltage and breakdown voltage of 228 V and 241 V respectively; dark current of 18 nA; responsivity of 65 A/W and a noise current of 0.2 pA/Hz. A transimpedance design was used because it offers a wide dynamic range and does not need equalization [5].

A schematic diagram of the preamplifier is given in Figure 5.2. The preamplifier consists of 3 stages. The first stage is a low gain common emitter amplifier. This is followed by a differential pair and finally a common collector stage. Bipolar transistors, each with an f_T of 4 GHz (BFR 90) were used for the active devices.

The first stage should have sufficient gain, so that noise generated by succeeding stages will be small when referred to the input of the first stage. Also it should have low input capacitance (C_i) since the bandwidth is inversely proportional to C_i. The mid-band gain of the first stage is approximately -2.3.

The differential pair provides adequate gain, and has a good high frequency response. The output impedance of the preamplifier is approximately 50 ohms to minimize reflections between the preamplifier and the main amplifier. The value of R_f determines the bandwidth and transimpedance of this circuit. The transimpedance is directly proportional to the value of R_f but the bandwidth is inversely proportional to it. The preamplifier had a bandwidth of about 100 MHz.

The preamplifier was constructed on a 4 cm x 5 cm printed circuit board which was enclosed in a die-cast metal chassis, with the APD mounted to one of its sides. High quality RF capacitors were used for decoupling the V_{cc} and APD bias voltage lines. Care was also taken to block stray RF energy from entering the preamplifier by using short, twisted pair wires with ferrite beads placed in series between the power supply and the preamp chassis.


+228 V
APD
C1
C2
R1
R2
C3
R3
R4
Q1
Q2
Q3
R5
R6
R7
R8
C4
Q4
C5
C7
R9
C6
R11
R10
C8
Rf
Cf

Q_1 - Q_4 - BFR 90
C_1 - 0.01 μF
C_2 - 46 pF
C_3, C_4, C_6 - 0.1 μF

C_5 - 10 μF
C_7 - 150 pF
C_f - 0.01 μF

R_1 - 270 KΩ
R_2 - 100 Ω
R_3, R_4, R_7, R_8 - 47 KΩ
R_5 - 680 Ω

R_6 - 560 Ω
R_9 - 220 Ω
R_{10} - 820 Ω
R_f - 3.3 KΩ

Fig. 5.2 Schematic Diagram of the Preamplifier [5]

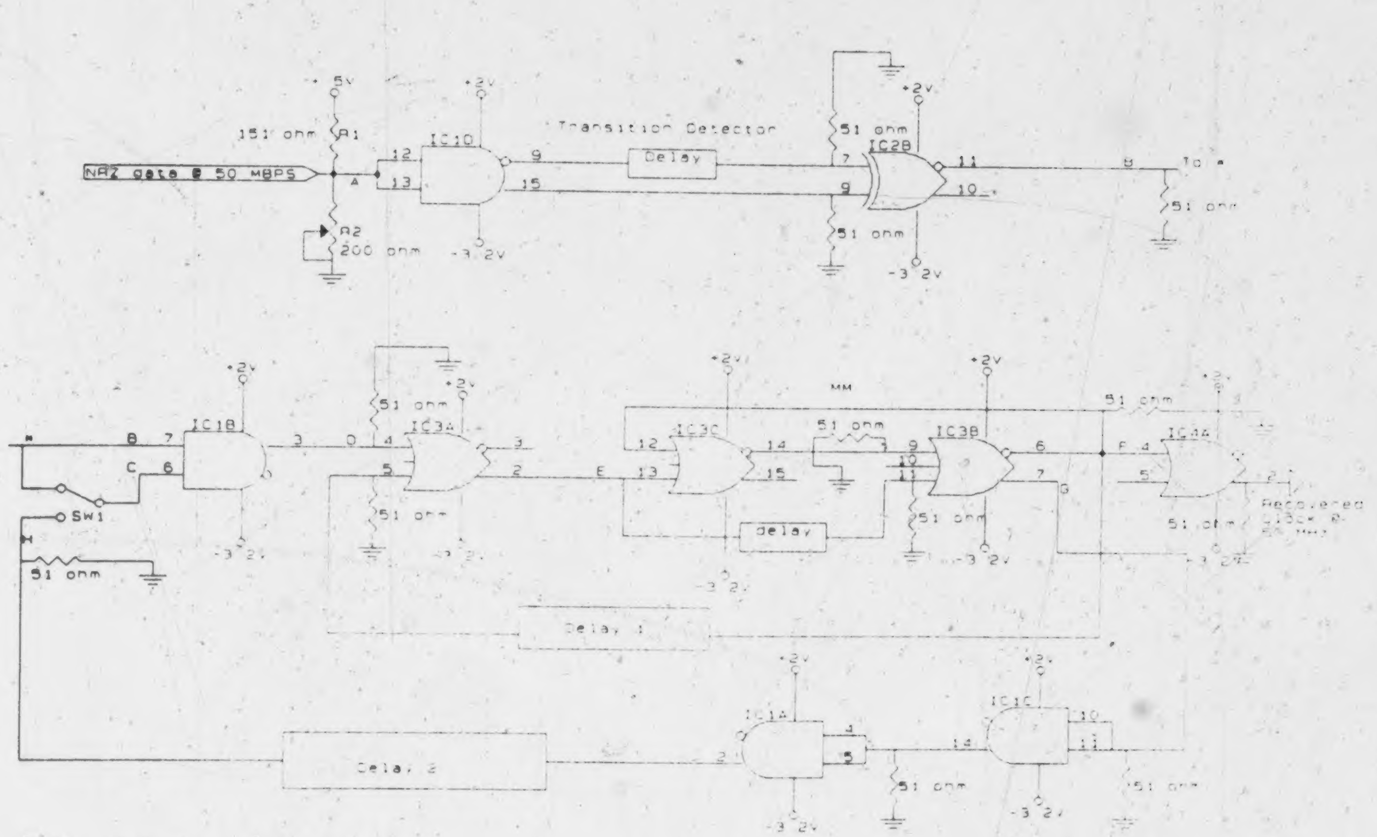
5.4 Main Amplifier

The output of the preamplifier is applied to a Keithley Instruments Pulse Amplifier (model 105). This amplifier provides a voltage gain of 100 (40 dB), has a bandwidth of 500 MHz, and an input impedance of 50 ohms. At low levels (around -48 dBm to -50 dBm) of optical power incident on the detector, the output of this amplifier is approximately 0.2 V peak-to-peak. Since this is too low to trigger ECL gates, it was amplified further by a HP 461A pulse amplifier, which has a voltage gain of 10 (20 dB) and a bandwidth of 150 MHz.

5.5 Clock Recovery Circuit

The self-sustaining monostable clock recovery circuit described in Chapter 3 was used to recover the clock signal from the incoming NRZ data. A schematic diagram of the experimental clock recovery circuit is shown in Figure 5.3. The original circuit developed by Witte and Moustakas [70] is obtained by connecting point C to point B and leaving point H open. The modified clock recovery circuit is obtained by joining point H to point C as shown in Figure 5.3.

The clock recovery circuit board has been designed for power supply voltages of +2 V and -3.2 V. This allows the 51 ohm resistors at the output of each gate to be returned to ground (0 V), with V_{EE} for each ECL chip equal to -3.2 V. The earlier threshold level of -1.3 V to trigger each ECL gate is now shifted to +0.7 V (+2 - 1.3). Since the optical receiver is ac coupled, the signal entering the clock recovery circuit is symmetrical about the 0 volt level (i.e. it has zero dc content), so that in order to trigger the ECL gates the received signal must be level shifted to +0.7 V. This level shifting is accomplished by resistors R1, R2 which form the components of a


NRZ gate @ 50 MBPS
+5V
151 ohm
R1
A
R2
200 ohm
IC1D
12
13
9
15
+2V
-3.2V
Transition Detector
Delay
51 ohm
IC2B
7
9
11
10
B
To
51 ohm
IC1B
B
C
7
6
3
SW1
51 ohm
D
4
5
IC3A
3
2
E
IC3C
12
13
14
15
delay
MM
IC3B
9
10
11
6
7
F
G
IC4A
4
5
2
Recovered
Clock @
50 MHz
Delay 1
Delay 2
IC1A
2
4
5
IC1C
14
10
11

IC1 - MC10H104
IC2 - MC10H107
IC3 - MC10H105
IC4 - MC10H103

Fig.5.3 Schematic Diagram of Clock Recovery Circuit

voltage divider circuit. The potentiometer R2 was adjusted to set point A to 0.7 V. At the same time, the values of R1 and R2 were chosen so that the effective resistance of R1 and R2 in parallel is about 50 ohms, thus minimizing reflections between the main amplifier and clock recovery circuit.

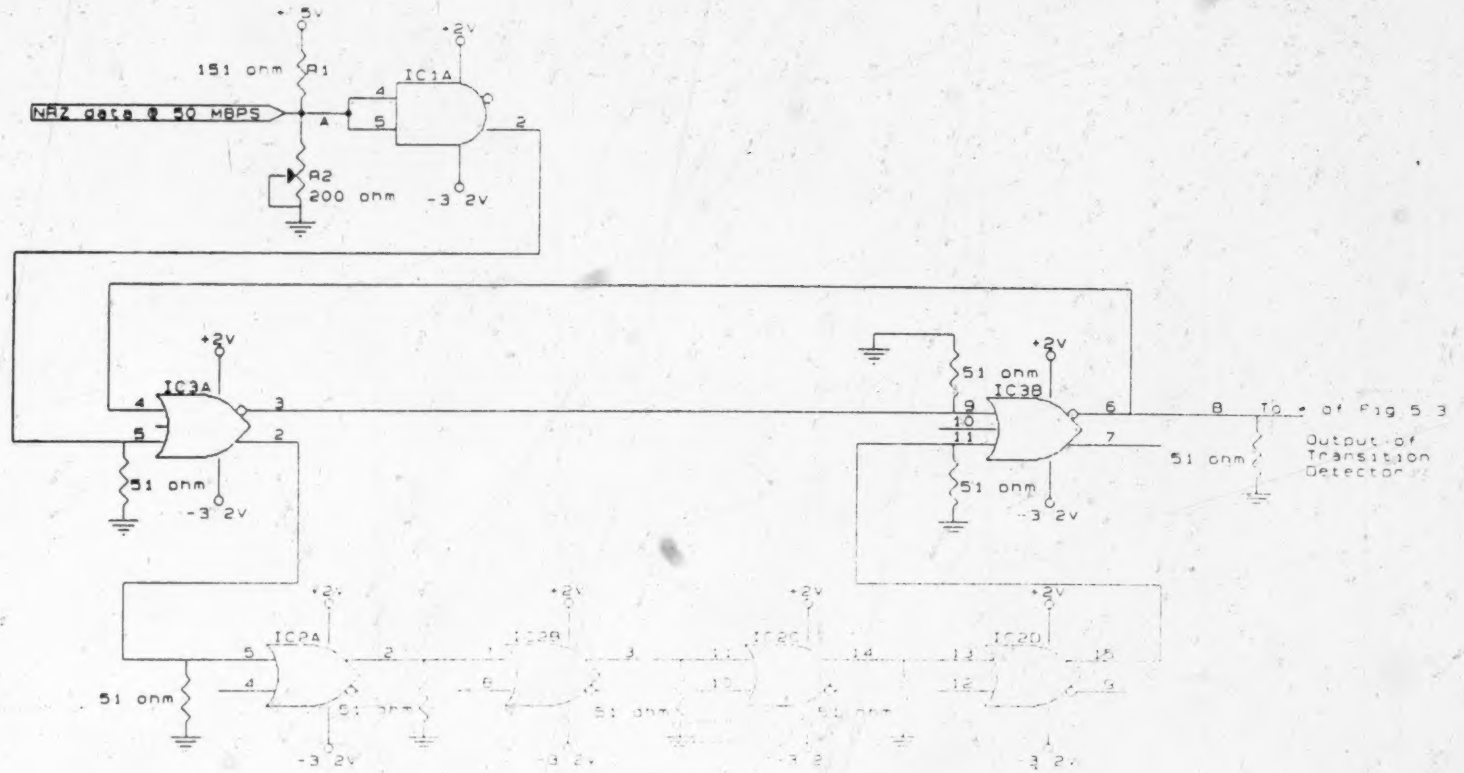
The incoming level-shifted signal is applied to the transition detector, which produces a ≅ 4 ns wide pulse at each rising and falling edge. The EX-OR and the transition detector form the non-linear element required to generate a spectral line at the incoming NRZ bit rate. The transition detector is realized by a NAND gate, an EX-OR gate, and a coaxial delay line (see Figure 5.3). On every input transition, a pulse is generated at the output of the EX-OR gate because its two inputs have unequal propagation delays (due to the delay line). The duration of the pulse is equal to the length of the delay. In the experimental system, a 0.78 m long coaxial delay line was used (RG 174/U). This corresponds to a pulse length of 3.9 ns, which is of sufficient duration to trigger the monostable multivibrator (MM).

The pulses from the transition detector, which will be referred to here as the primary pulses, are fed to an AND gate (IC 1B). If the original clock recovery circuit is desired, both the inputs to this gate are tied together and hence its output will be equal to its input. However, for the modified circuit, the transition detector output is gated (by an AND gate) with the delayed clock output (delay < T), so that, triggering of the MM by pulses that arrive too early is inhibited. Whenever this occurs, the MM will be triggered by the delayed clock pulse. Since this occurs closer to the ideal time, a reduction of overall clock jitter can be obtained. The output of the AND gate forms one of the inputs to an OR gate (IC 3A). The other input to the OR gate is the output clock signal delayed by the inner feedback loop by T1 seconds (T1 > T). If the primary pulse is late or missing, this delayed clock signal will trigger the MM.

The monostable multivibrator (MM) is realized by logic gates [88]. It produces a 5.0 ns pulse on every rising edge of its input signal. The output of the MM is at 50 MHz (the NRZ input bit rate).

When the input to the clock recovery circuit is left open, the circuit oscillates at a free running frequency of 1/T1. This oscillation is started by a transient pulse triggering the MM when the power is turned on. Due to the inner feedback, the MM is then repeatedly triggered every T1 seconds. By measuring the frequency of oscillation (using an HP 5326A Timer-Counter), the exact value of the delay T1 can be established. The frequency of oscillation changes by a few hundreds of KHz, when the +2 V power supply is adjusted slightly. This occurs because the amplitude of the gate outputs are changed slightly, resulting in changes in effective gate delay times due to amplitude-to-phase conversion that occurs because of non-zero gate thresholds. When the input to the clock recovery circuit is connected, the frequency of oscillation locks on to the bit rate of 50 MHz.

A new version of the modified MM clock recovery circuit was later developed due to the reasons mentioned in Sections 3.3.1 and 4.1.2. The only change compared to Figure 5.3 is in the transition detector. The NAND gate and the EX-OR gate were replaced by a MM (see Figure 5.4). It triggers only on the rising edge of the incoming level-shifted signal. Thus, we have pulses at the output of the


+5v
151 ohm
R1
NRZ data @ 50 MBPS
A
R2
200 ohm
+2v
IC1A
4
5
2
-3.2v
+2v
IC3A
4
5
3
2
51 ohm
-3.2v
51 ohm
+2v
IC3B
9
10
11
6
7
51 ohm
-3.2v
8
To • of Fig 5.3
51 ohm
Output of
Transition
Detector
+2v
IC2A
5
4
2
51 ohm
-3.2v
+2v
IC2B
7
6
3
51 ohm
-3.2v
+2v
IC2C
11
10
14
51 ohm
-3.2v
+2v
IC2D
13
12
15
9
-3.2v
51 ohm

IC1 - MC10H104
IC2 - MC10H103
IC3 - MC10H105

Fig.5.4 Schematic Diagram of Transition Detector

transition detector only on the rising edge of the input signal. These pulses have a duration equal to 4ns (the propagation delay of the four OR gates IC 2A to IC 2D).

Both clock recovery circuits were constructed on 15 cm x 10 cm PC boards. Delay 1 was realized by a 3.4 m coaxial line (RG 174/U), whose delay of approximately 16 ns together with the propagation delay of the gates make T1 = 20.033 ns. Delay 2 was realized with two AND gates and a 3.5 m coaxial line (T2 = 19.88 ns). Coaxial BNC connectors (50 ohm) were used at the input and the output. Circuit interconnections were kept as short as possible. In order to avoid problems due to reflections, fifty ohm microstrip transmission lines were used throughout. Power supply lines on the pc board were decoupled to ground by high quality RF (mylar) capacitors (0.1 μf, 47 pf and 100 μf) at several points.

Most of the jitter measurement experiments and analysis were done only with the original monostable clock recovery circuit. Referring to Figure 5.3, the inputs to the AND gate (IC 1B) were tied together and the feedback loop of delay 2 was not used. The main objective of this thesis was to develop a suitable technique to measure the timing jitter on a bit-by-bit basis. The jitter of the self-sustaining monostable clock recovery circuit was later measured using this measurement technique.

5.6 Jitter Measurement System

The experimental system used to measure timing jitter on a bit-by-bit basis is illustrated in Figure 5.5. It consists of a HP54201A digitizing oscilloscope connected to a HP-85 computer through a Hewlett Packard Interface Bus (IEEE-488 Bus). The HP-85 serves as a

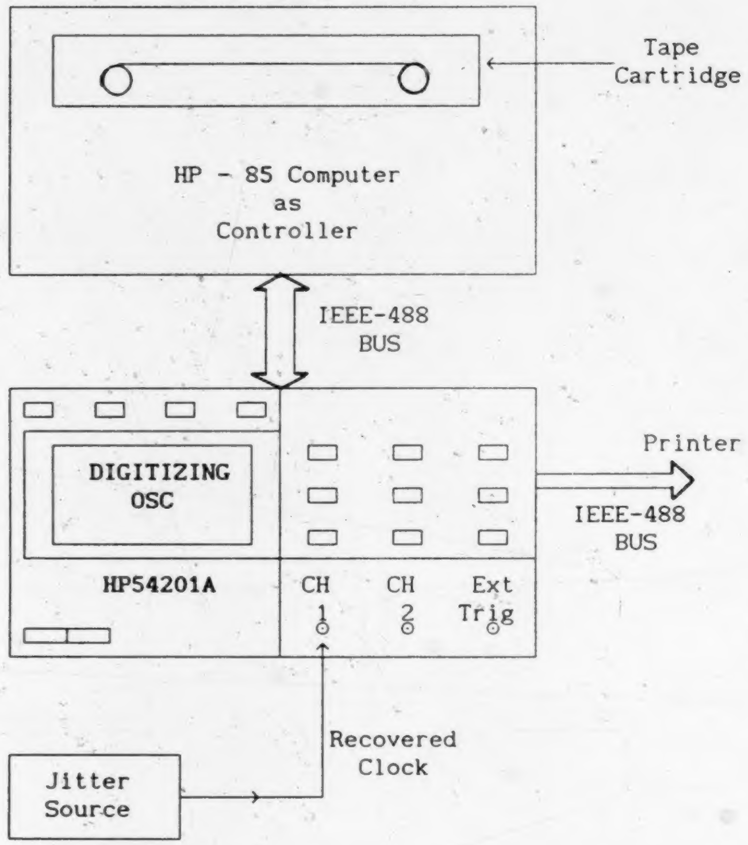

Tape
Cartridge
HP - 85 Computer
as
Controller
IEEE-488
BUS
DIGITIZING
OSC
HP54201A
CH
1
CH
2
Ext
Trig
Printer
IEEE-488
BUS
Recovered
Clock
Jitter
Source

Fig. 5.5 Experimental Jitter Measurement System

controller. It has been programmed to automatically acquire a waveform and store the digitized data on the tape cartridge. The data can also be transferred to a printer which is connected to the digitizing oscilloscope through an IEEE-488 bus.

The HP54201A is a dedicated, two channel, waveform-acquiring digital storage oscilloscope with full HP-IB programmability, and digitized waveform data output. It has a 300 MHz repetitive bandwidth and a single-shot digital storage bandwidth of 50 MHz (200 Megasamples/second). In the real-time sampling mode, the sample rate depends on the time range selected. For example, using the 10 μs time range (1 μs/cm) the sample rate is 100 Mega Samples/second. The scope can acquire a maximum of 1000 samples on each acquisition, on a single-shot basis. The minimum input voltage range is 40 mV (5 mV/cm). It has a vertical resolution of 6 bits. Hence, the maximum number of quantization levels is 64 (2^6).

As an indication of the ultimate resolution attainable with this equipment, the lowest jitter level that can be measured for a signal slope of 3.684×10^8 is (using equation (4.2))

$$\Delta t = \frac{40 \text{ mV}/ 64 \text{ levels}}{3.684 \times 10^8} = 1.7 \text{ ps}.$$

The measurement technique has been discussed in detail in Section 4.3. The ultimate accuracy of the scheme is limited by the temporal and vertical resolution, and the stability of the sampling, triggering and DC offset circuitry of the oscilloscope. It should be noted that the peak-to-peak jitter range is limited to the linear rise time of the signal. If the jitter exceeds this limit then samples may be taken on the falling edge, in which case the results will not be correct.

The greatest problem found in using the digital processing oscilloscope (DPO) is that it critically depends on the operator settings. The trigger level and the sensitivity controls have to be adjusted to give a stable signal on the display. The trigger level and the delay have to be manually optimized until a good response is obtained. This leads to difficulty in repeating the results.

In the next chapter we present the system operation and waveforms at various points of the experimental fiber optic system. The experimental jitter measurement results are also presented and discussed.

CHAPTER 6

EXPERIMENTAL RESULTS AND DISCUSSION

e experimental optical fiber communication system employing the NRZ code, described in the previous chapter, was set up and various measurements were made. The overall system specifications are given in Table 6.1. The relationship between the RMS jitter and the received optical power level, for various transmitted bit patterns were obtained. The performance of the optical receiver, clock recovery circuit and the jitter measurement system are presented first. Next, the experimental relationship between the systematic RMS jitter, total RMS jitter and the transmitted bit patterns are discussed. Finally, the relationship between the total RMS jitter and received optical power level is discussed, with respect to various data patterns and pseudo-random bit sequences.

An examination of these results will be useful in understanding the jitter performance of the self-sustaining monostable multivibrator clock recovery circuit. The results also enable us to obtain the jitter statistics, which are useful in determining the performance of an optical communication system in the presence of timing jitter.

6.1 System Operation and Waveforms

6.1.1 Data Generator

Figure 6.1 illustrates the output waveform of the data generator. It is an NRZ 16-bit repetitive sequence of 1001001001001001 at 50 Mb/s. This signal modulates the laser transmitter. As the input impedance of the laser driver amplifier is 50 ohm and requires an RF input of less than 20 mA peak-to-peak for 50% modulation depth, the amplitude of the output of the data generator is adjusted for 0.8 V peak-to-peak.

Table 6.1 System Specifications

Parameters	Specifications
Data rate	50 Mbits/s
Type of line code	NRZ
Source type	Laser Diode
Source wavelength	830 nm
Source spectral width	0.84 nm
Fiber type	Graded index Multimode fiber
Fiber attenuation	2.75 dB/km
Fiber dispersion	1.5 ns/nm-km
Length of the fiber	5 km
Bandwidth-distance product	246.83 MHz-km
Power coupled into the fiber	-20 dBm
Detector type	APD

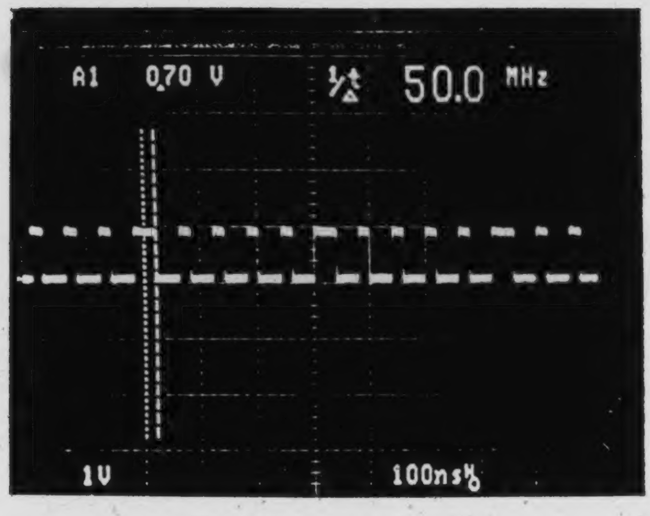


Fig. 6.1 NRZ Data Pattern of 1001001001001001 at the Output of the Data Generator.

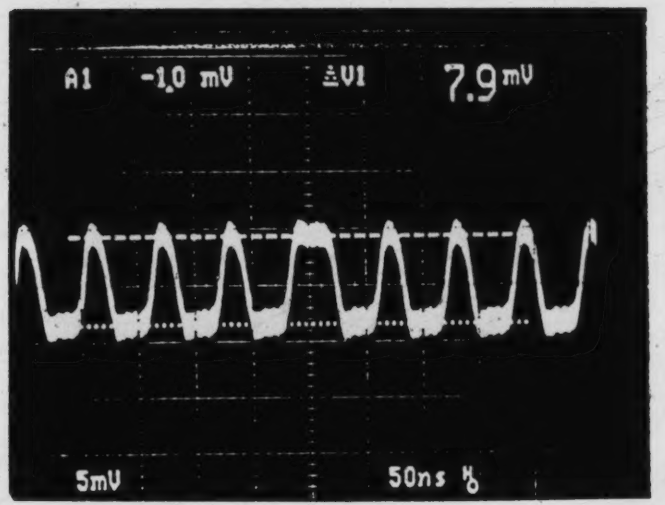


Fig. 6.2 Output of the APD detector/Pre-amplifier
Transmitted Data Pattern: 1001001001001001
Received Optical Power : -42 dBm

6.1.2 Optical Receiver and Main Amplifier

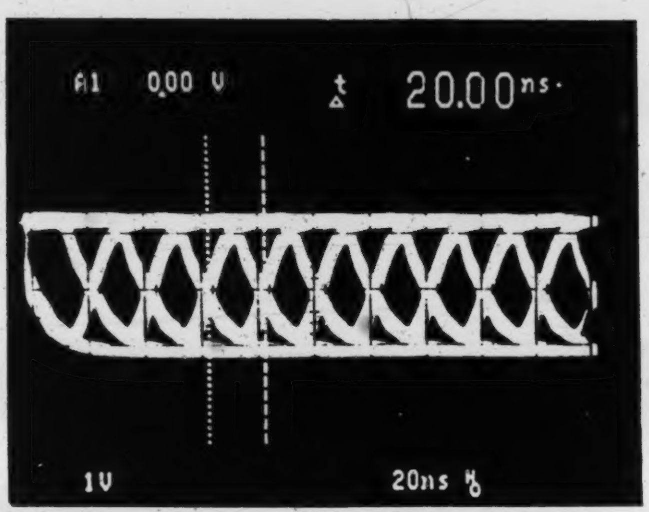
Figure 6.2 shows the signal at the output of the preamplifier for the same transmitted data pattern as mentioned in the above section. The optical power level at the receiver is -42 dBm.

Figures 6.3 (a) and (b) show the eye diagram at the output of the main amplifier for an NRZ pseudo-random bit sequence (of length $2^{23}-1$) applied to the laser transmitter, at received optical power levels of -35.8 and -50.5 dbm, respectively. For these diagrams, the low pass filter at the output of the preamplifier, i.e. the capacitor C8 (Fig. 5.2), is removed. Note in Fig. 6.3 (a), that the eye diagram is skewed slightly. This might be due to the large amount of optical power falling upon the detector. However, the eye is open in both cases, which implies that the fiber-receiver bandwidth is sufficient for a signalling rate of 50 Mb/s. The transimpedance of the preamplifier circuit is approximately 1980 ohms (into a 50 ohm load). The 3 dB bandwidth of the receiver, with C8 absent, is approximately 65 MHz [5].

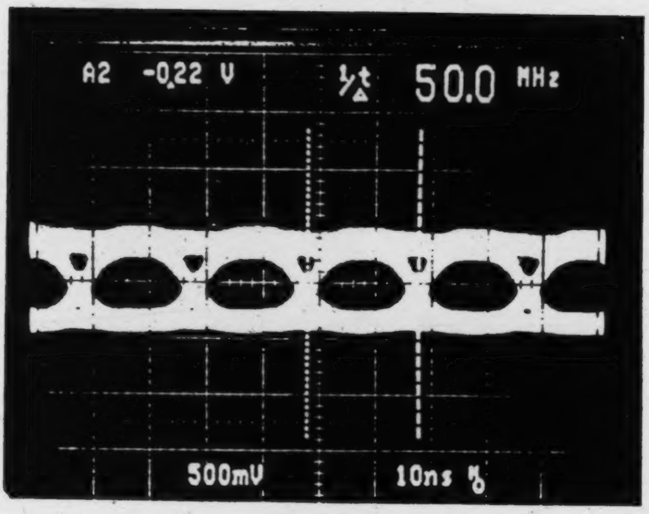
6.1.3 Clock Recovery Circuit

Figure 6.4 demonstrates the operation of the original self-sustaining monostable multivibrator clock recovery circuit (refer to Fig. 5.3). The input signal to the clock recovery circuit is a 16-bit repetitive NRZ sequence of 1001001001001001 at a received optical power level of -49 dBm, as shown in Fig. 6.4 (a). The output of the original clock recovery circuit, for this input is shown in Fig. 6.4 (b).

The operation of the new version of the original monostable clock recovery circuit (Fig. 5.4) is demonstrated in Fig. 6.5. The input to the clock recovery circuit is a 16-bit repetitive NRZ sequence of



(a)



(b)

Fig. 6.3 Eye diagram at the output of the main amplifier for an NRZ pseudorandom bit sequence $2^{23}-1$ for received optical power levels of a) -35.8dBm b) -50.5dBm

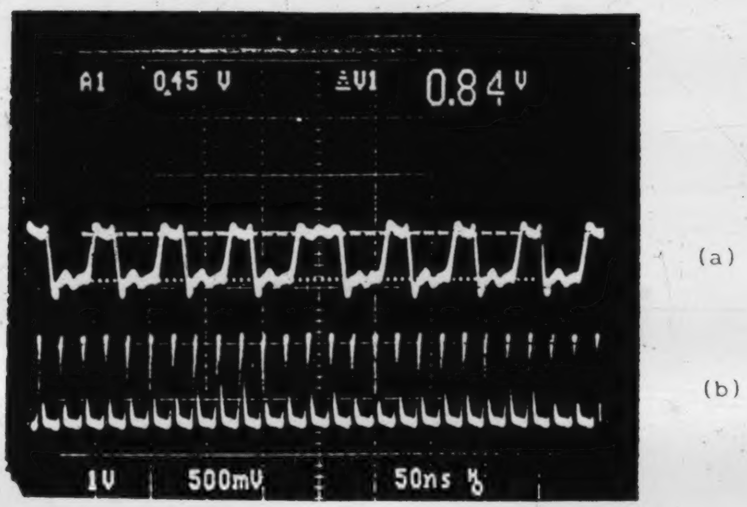


Fig. 6.4 Clock Recovery Circuit Waveforms
(a) Input (Received Optical Power = -49 dBm, NRZ sequence 1001001001001001)
(b) Output of the Original Clock Recovery Circuit (Δ = 0.033 ns)

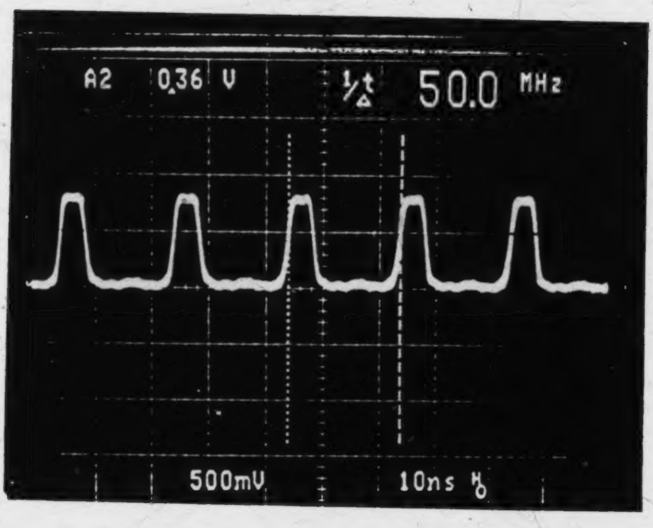


Fig. 6.5 Output of the New Version of the Original Clock Recovery Circuit
(Input = NRZ sequence of 1010101010101010 at Received Optical Power of -45 dBm, Δ = 0.033 ns)

1010101010101010 at a received optical power level of -45 dBm. The slope of the signal as measured on the analog oscilloscope (Tektronix 2465) is 3.68 x 10^8 (0.7 V/ 1.9 ns).

It was observed while performing the measurements that, as the received optical power level was varied, the potentiometer R2 of the DC level shifter (refer to Fig. 5.3) had to be adjusted for proper operation of the clock recovery circuit. The reason for this behaviour is that when the received optical power is changed, the amplitude of the main amplifier output changes, since automatic gain control (AGC) is not incorporated in the optical receiver. This amplitude change results in a slight phase shift in the output of the EX-NOR gate (IC2B, see Figure 5.3) due to the incoming signal crossing the ECL gate threshold at a slightly different time. This phenomenon is more commonly referred to as amplitude-to-phase conversion. This problem could be overcome by employing an amplifier which delivers an output of constant amplitude and phase shift for a large dynamic range of the input signal.

The recovered clock is applied next to the jitter measurement system. The results of the jitter measurement will be discussed in Section 6.2.

6.1.4 Jitter Measurement System

The output of the clock recovery circuit is applied to the experimental jitter measurement system (see Fig. 5.5). The clock is recovered using the new version of the monostable circuit. The recovered clock signal is applied to channel 1 of the digitizing oscilloscope. The oscilloscope is set for the following conditions:

Sample rate: 100 MSamples/sec. (10 μs time range) real-time sampling mode.

Amplitude range: 93.8 mV/div.

DC Offset: 350 mV.

Trigger source: Channel 1

Trigger slope: Positive

Trigger level: 50% of peak-to-peak amplitude

Figures 6.6 (a), (b), (c), (d) and (e) illustrate the acquired patterns as seen on the screen of the digitizing oscilloscope for the 16-bit repetitive data sequences, 1010101010101010, 1000100010001000, 1000000010000000, 1000000000000000 and for PRBS $2^{23}-1$, respectively. Figures 6.7 (a), (b), (c), (d) and (e) illustrate the corresponding histogram estimate for the probability density function of the recovered clock timing jitter obtained from Equation (4.3). The amplitude scale of the oscilloscope in volts shown in Figures 6.6, is converted to the time scale using Equation (4.2).

In Figures 6.7(a) to 6.7(d), the vertical bar to the right and the vertical bars to the left represent the time of occurrence of the recovered clock when the clock recovery circuit (Fig.5.3) is triggered by the primary pulses and by the feedback pulses, respectively. The clock recovery circuit is triggered by the primary pulses whenever there is a positive transition in the input data to the clock recovery circuit, and by the feedback pulses in the absence of a positive transition, for each bit interval T.

Note from Fig.6.7(a), that the recovered clock due to the feedback pulses occurs 0.095 seconds after the ideal time. Theoretically, the recovered clock should occur only Δ seconds (≅ 0.033 ns) later than the

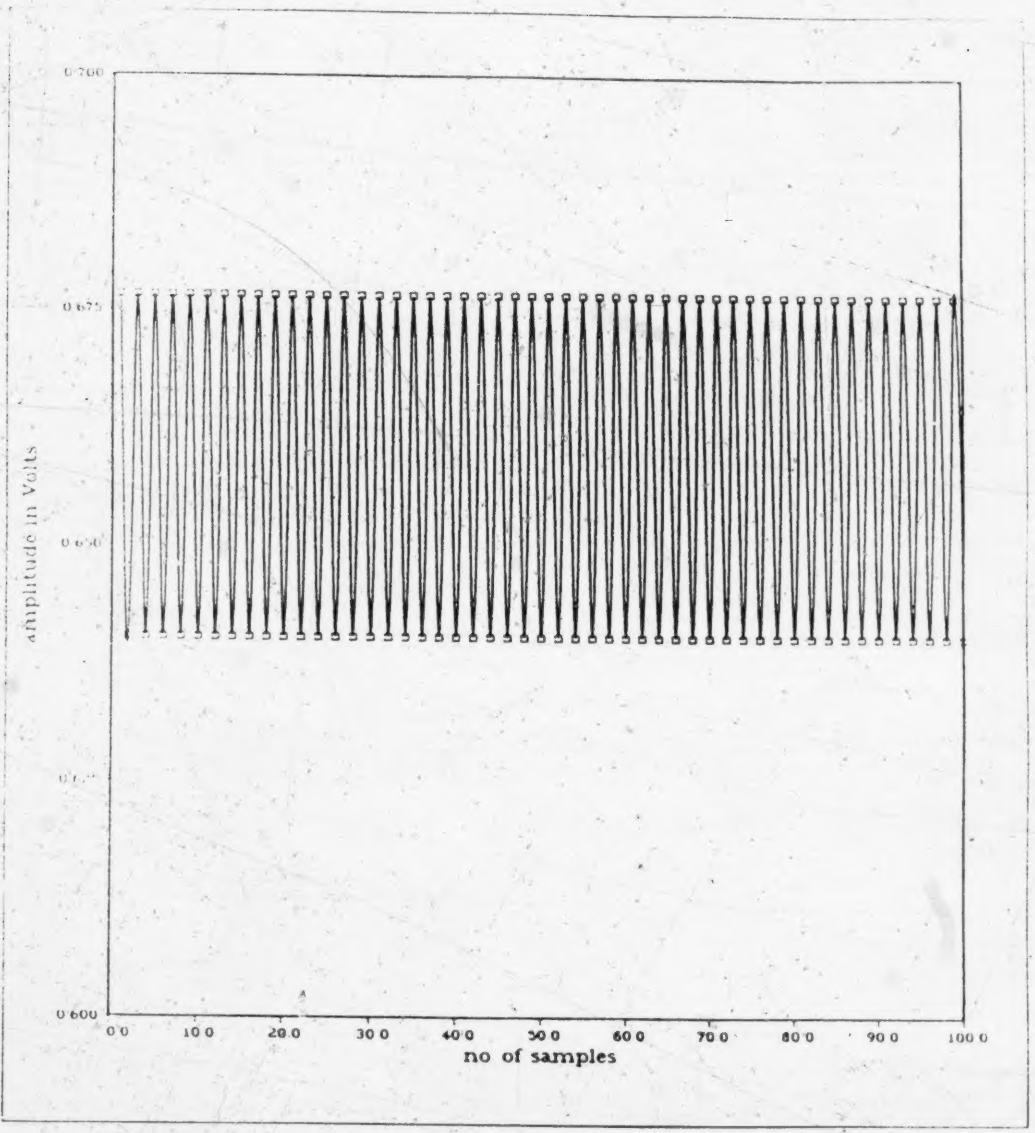


Fig. 6.6(a) Pattern of Occurrence of the Recovered Clock as seen on the Screen of the Digitizing Oscilloscope for a 1010101010101010 Data Pattern applied to the Input of the Clock Recovery Circuit.

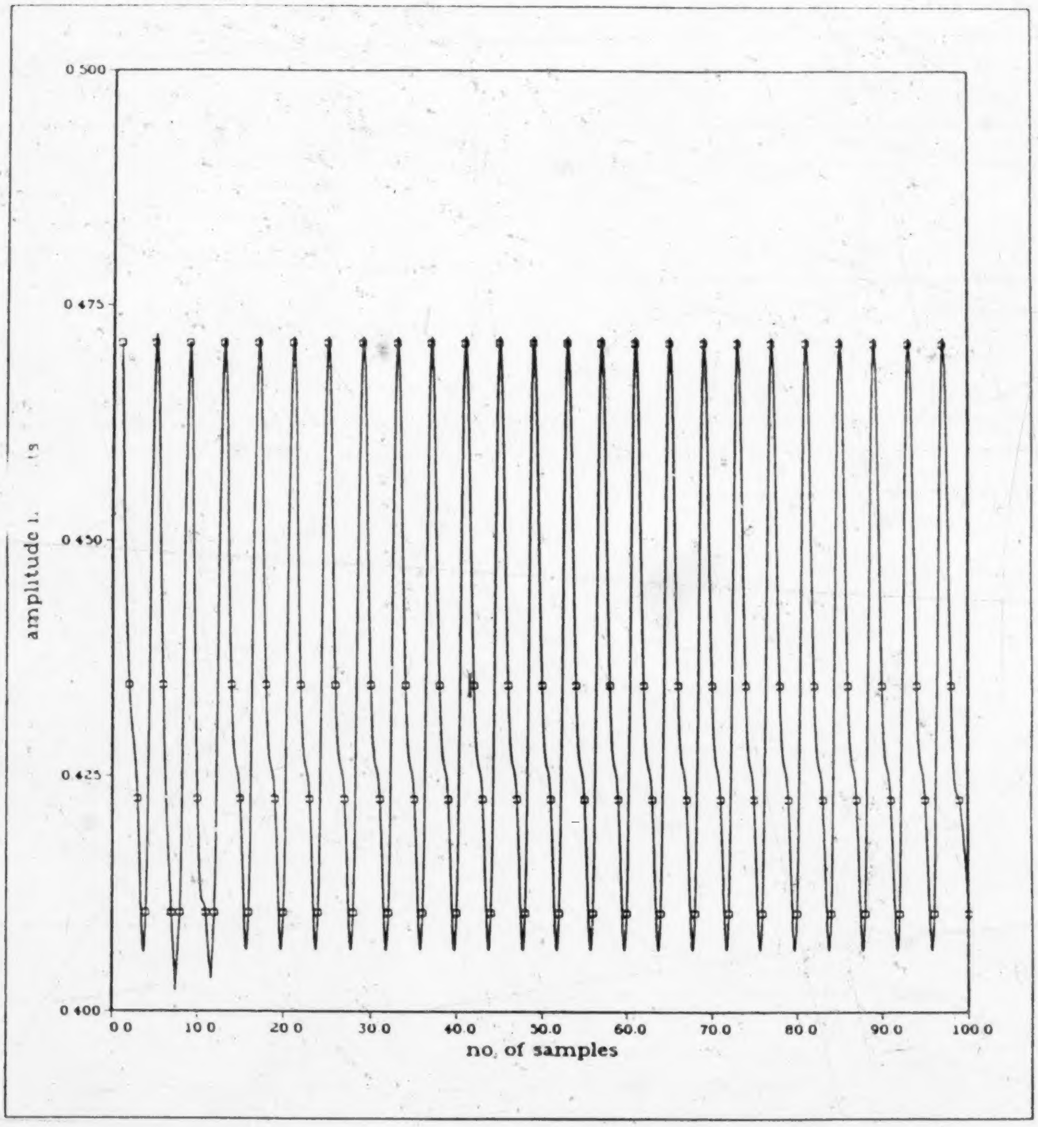


Fig. 6.6(b) Pattern of Occurrence of the Recovered Clock as seen on the Screen of the Digitizing Oscilloscope for a 1000100010001000 Data Pattern applied to the Input of the Clock Recovery Circuit.

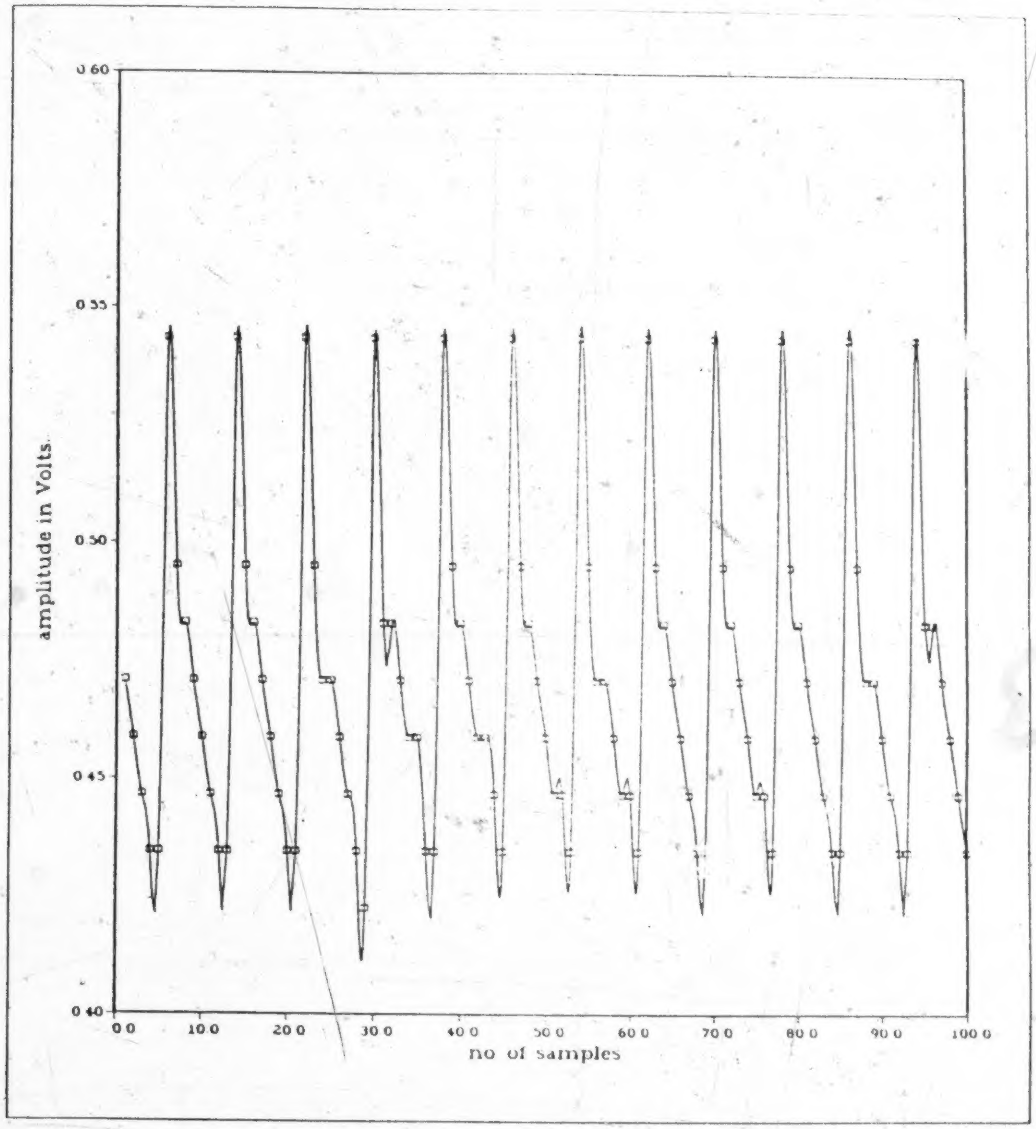


Fig. 6.6(c) Pattern of Occurrence of the Recovered Clock as seen on the Screen of the Digitizing Oscilloscope for a 1000000010000000 Data Pattern applied to the Input of the Clock Recovery Circuit.

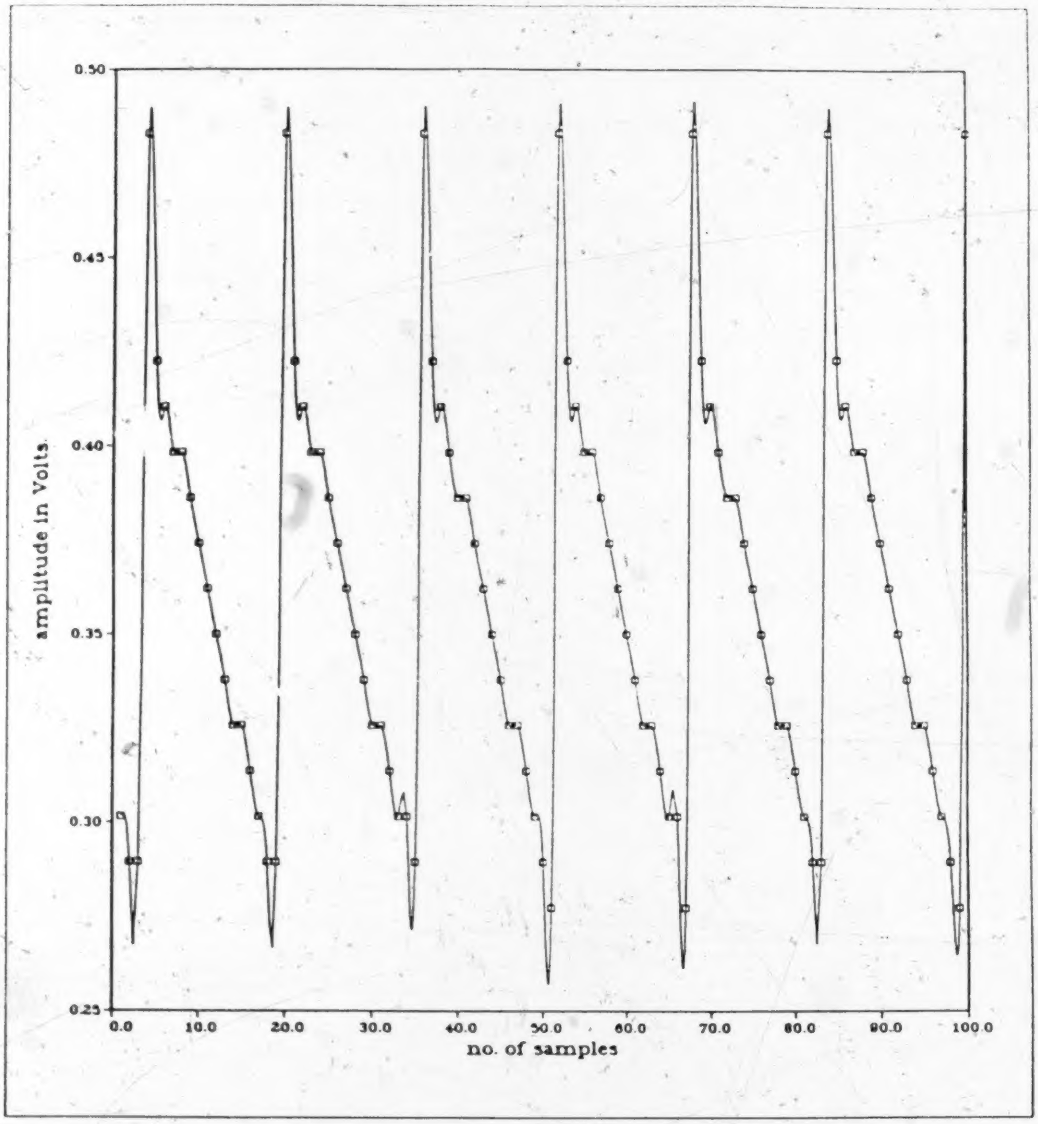


Fig. 6.6(d) Pattern of Occurrence of the Recovered Clock as seen on the Screen of the Digitizing Oscilloscope for a 1000000000000000 Data Pattern applied to the Input of the Clock Recovery Circuit.

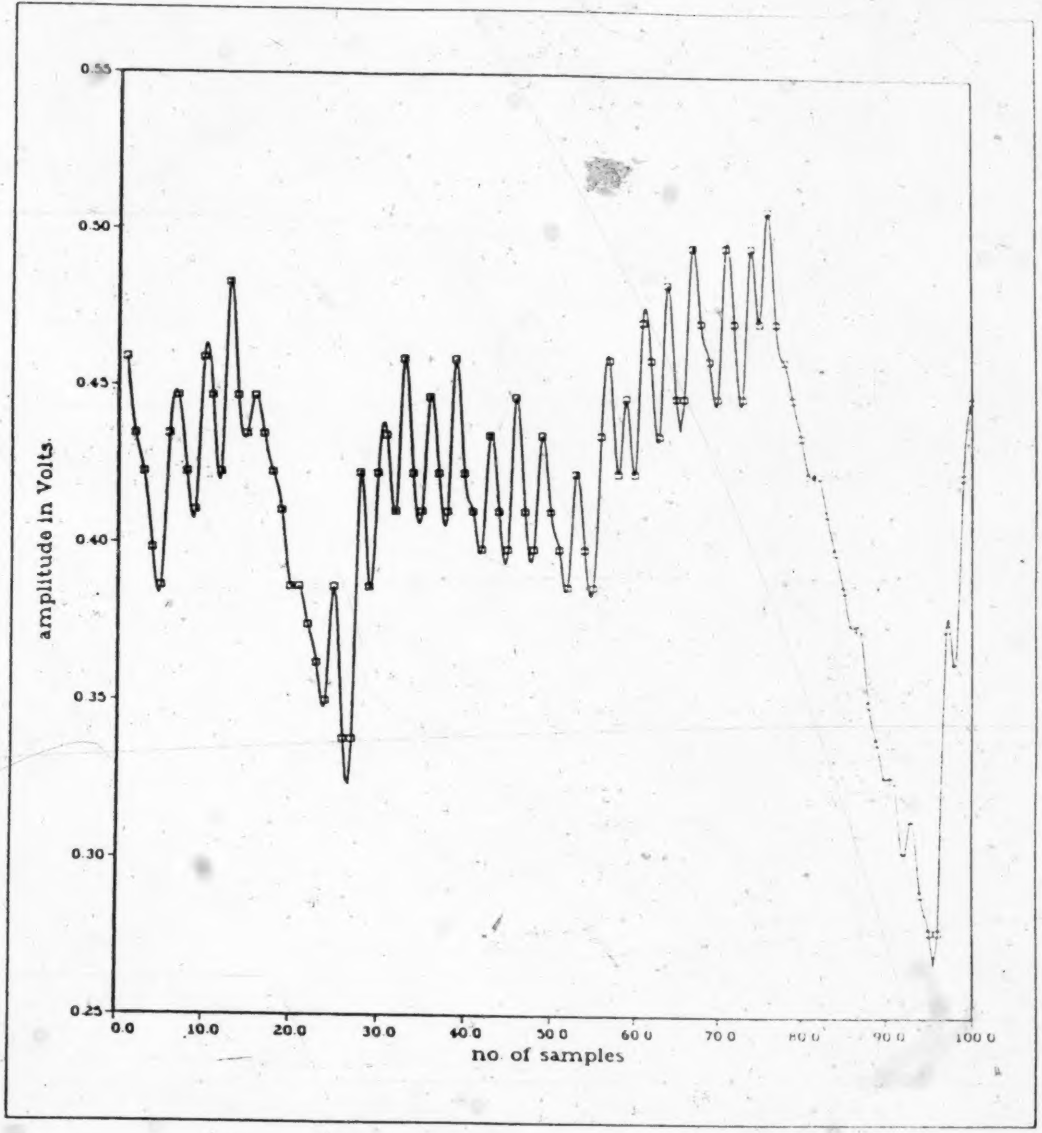
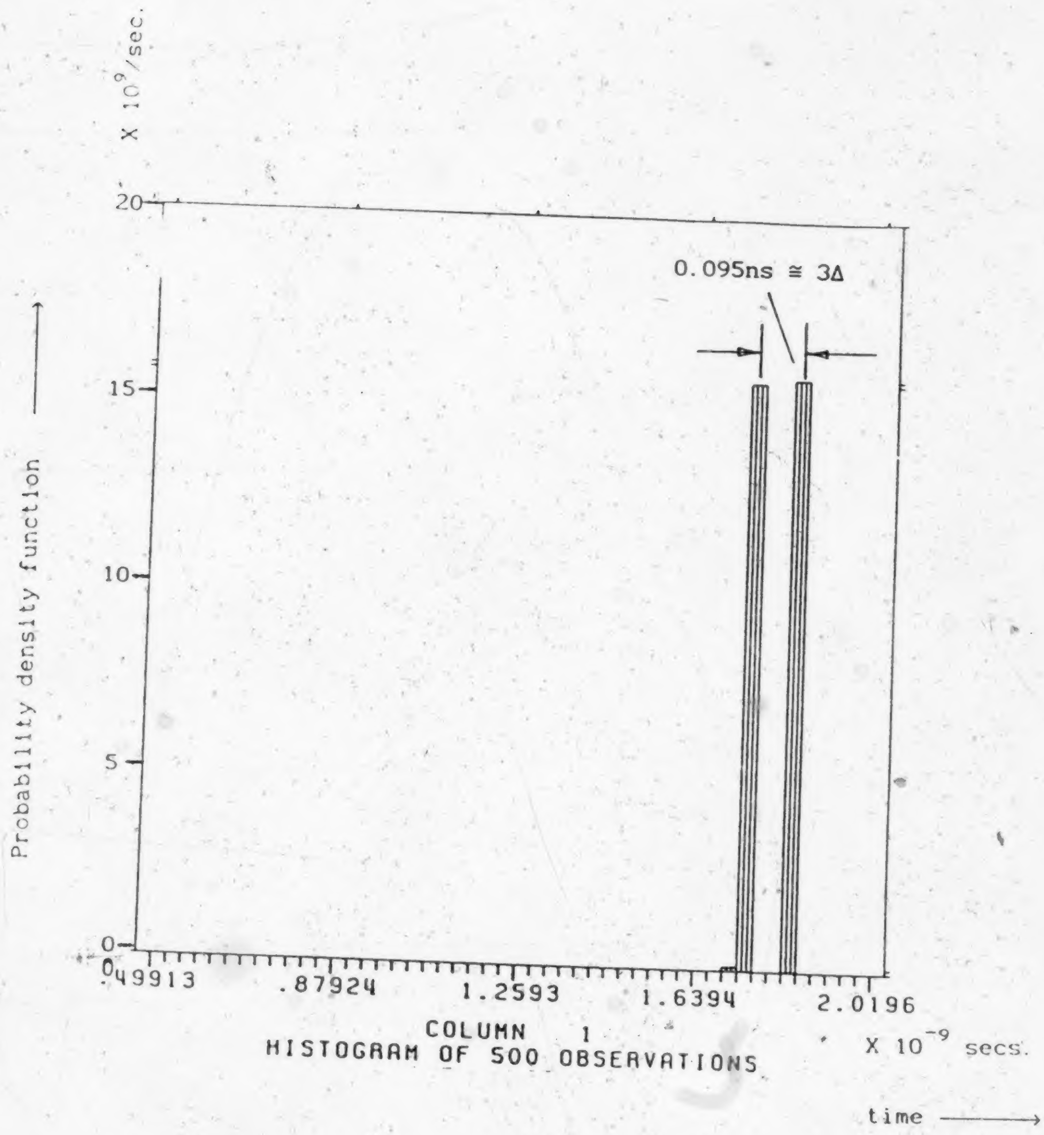
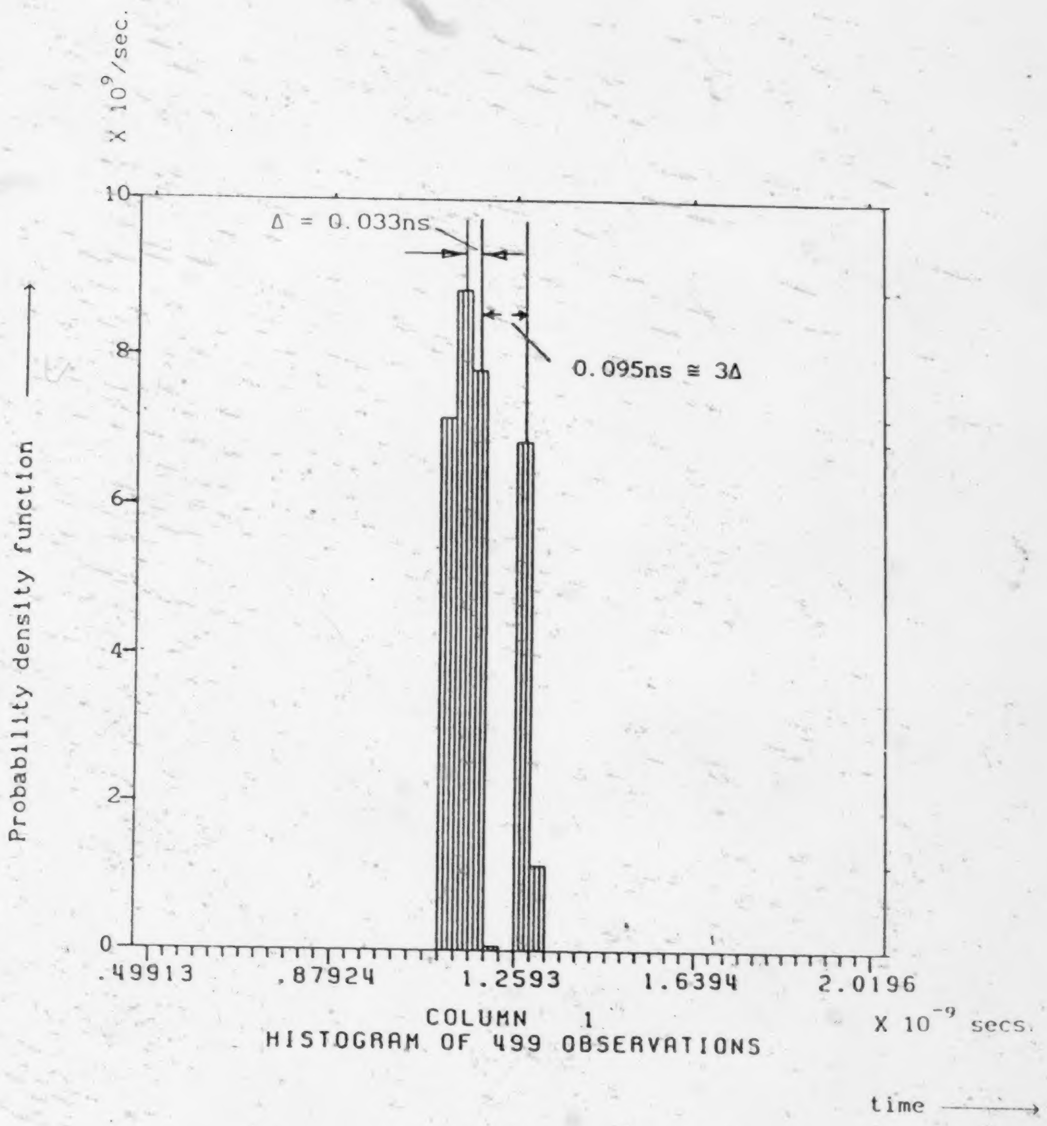


Fig. 6.6(e) Pattern of Occurrence of the Recovered Clock as seen on the Screen of the Digitizing Oscilloscope for a PRBS 2^{23} - 1 Data Pattern applied to the Input of the Clock Recovery Circuit.



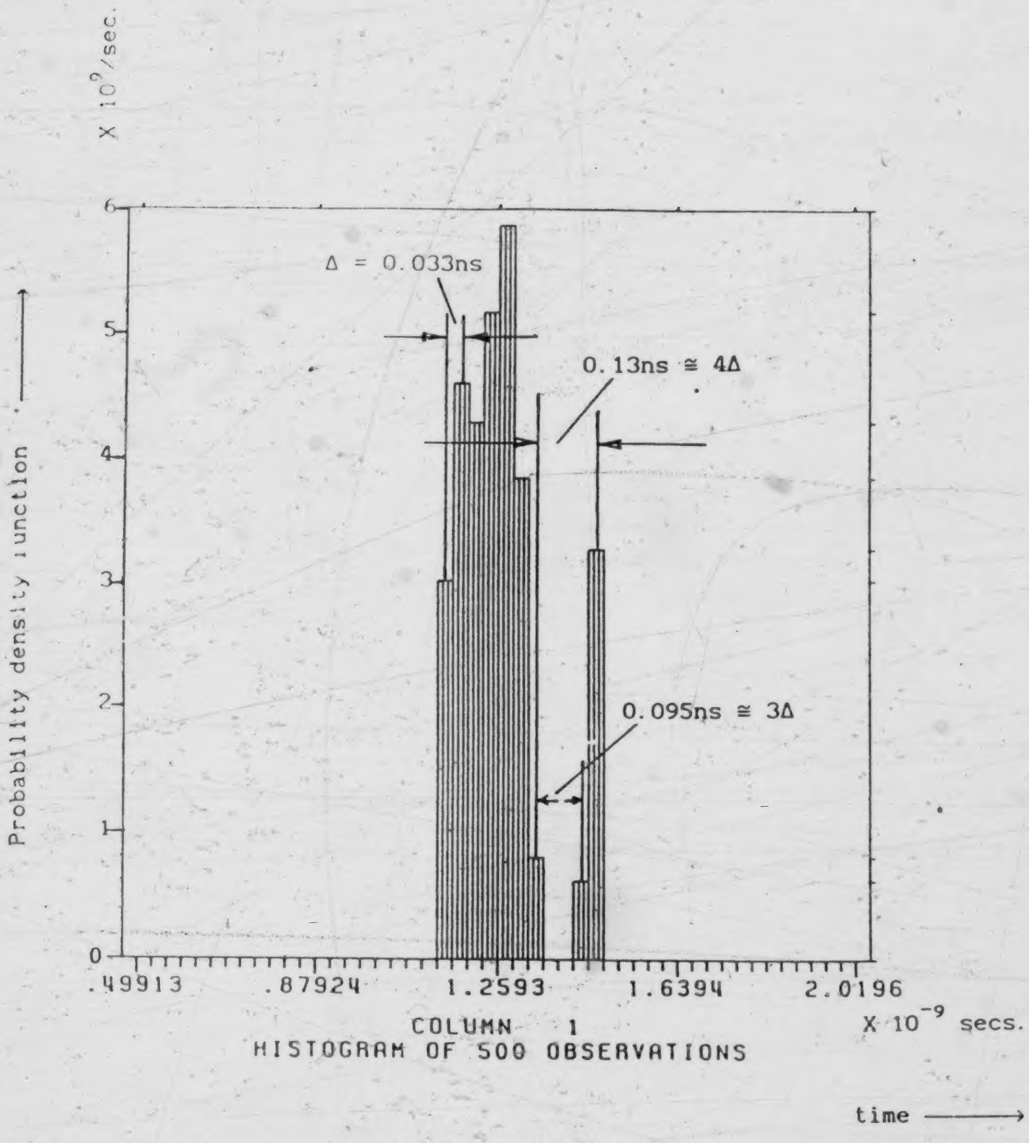
MEAN = 1.7892 ns STANDARD DEVIATION (σ) = 0.049 ns

Fig. 6.7(a) **Histogram Estimate for the Pdf of the Recovered Clock Timing Jitter when a 1010101010101010 Data Pattern is applied to the Input of the Clock Recovery Circuit.**



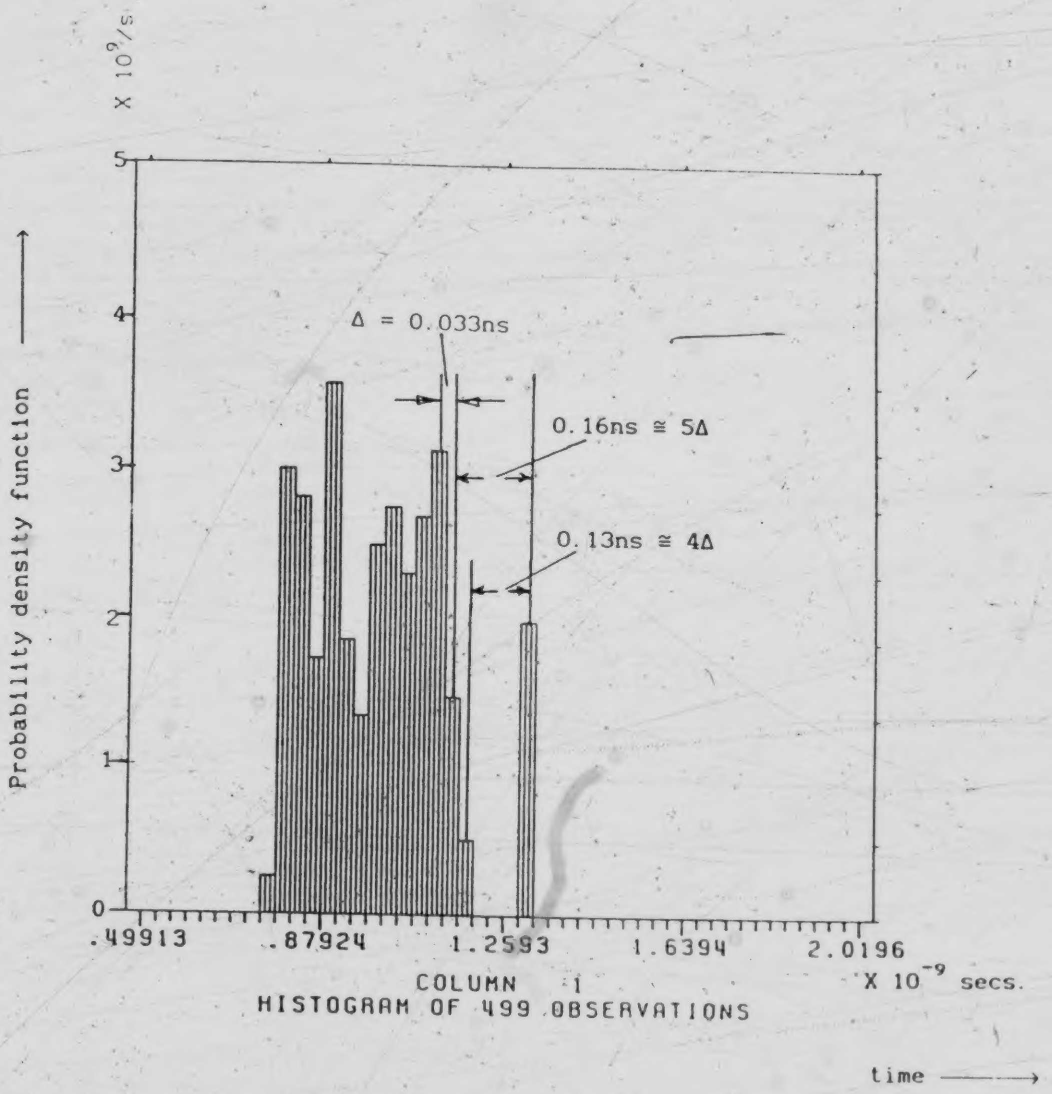
MEAN = 1.1832 ns STANDARD DEVIATION (σ) = 0.063 ns

Fig. 6.7(b) Histogram Estimate for the Pdf of the Recovered Clock Timing Jitter when a 1000100010001000 Data Pattern is applied to the Input of the Clock Recovery Circuit.



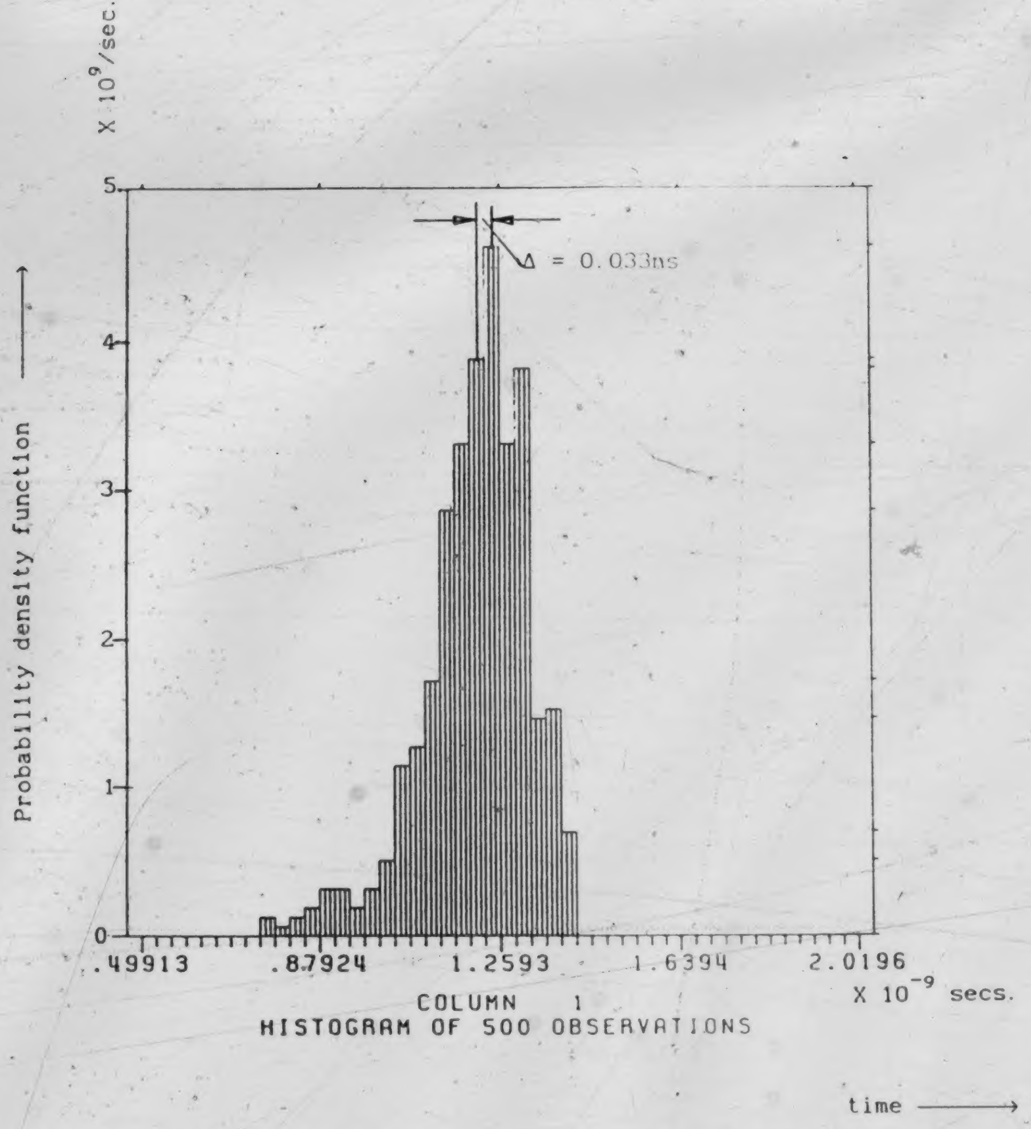
MEAN = 1.2680 ns STANDARD DEVIATION (σ) = 0.093 ns

Fig. 6.7(c) Histogram Estimate for the Pdf of the Recovered Clock Timing Jitter when a 1000000010000000 Data Pattern is applied to the Input of the Clock Recovery Circuit.



MEAN = 0.9856 ns STANDARD DEVIATION (σ) = 0.143 ns

Fig.6.7(d) Histogram Estimate for the Pdf of the Recovered Clock Timing Jitter when a 1000000000000000 Data Pattern is applied to the Input of the Clock Recovery Circuit.



MEAN = 1.2102 ns STANDARD DEVIATION (σ) = 0.117 ns

Fig.6.7(e) Histogram Estimate for the Pdf of the Recovered Clock Timing Jitter when a PRBS $2^{23}-1$ Data Pattern is applied to the Input of the Clock Recovery Circuit.

ideal time, since the feedback delay is greater than the bit interval T (20 ns) by that amount. Thus a 1 to 0 transition gives much too long a delay. Observing Figures 6.6(b) and 6.7(b) we again note that, when there is a transition from 1 to 0 in the input data to the clock recovery circuit, or in other words, when the clock recovery circuit is triggered by a primary pulse and a feedback pulse in succession, the recovered clock pulses are not separated by Δ seconds but by a significantly longer time. However, when the clock recovery circuit is triggered only by the feedback pulses, the recovered clock pulses are separated by Δ seconds in time as expected. A similar phenomenon is observed in Figures 6.7(c) and 6.7(d), except that the separation between the recovered clock pulses due to a primary pulse and a feedback pulse is about 0.13 ns and 0.16 ns, respectively.

Thus, in general, from Figures 6.7(a) to 6.7(e), the measured results show that when the clock recovery circuit is triggered by a primary pulse and then by a feedback pulse, the time interval between the two recovered clock pulses is greater than T1 (T+Δ) seconds. On the other hand, when the clock recovery circuit is triggered only by the feedback pulses the recovered clock pulses occur every T1 seconds.

In order to verify the above statement, the time interval between the recovered clock pulses was measured directly on the oscilloscope for different, 16-bit data patterns applied to the input of the clock recovery circuit. The results are shown in Table 6.2.

Table 6.2

Transmitted bit sequence (16-bit repetitive pattern)	Measured time interval between two successive recovered clock pulses when the input data to the clock recovery circuit		
	has a 0 to 1 transition	has a 1 to 0 transition	has no transitions
1010101010101010	19.73 ± 0.05ns	20.39 ± 0.05ns	-----
1000100010001000	19.68 ± 0.04ns	20.28 ± 0.04ns	20.08 ± 0.05ns
1000000010000000	19.55 ± 0.05ns	20.28 ± 0.03ns	20.08 ± 0.05ns
1000000000000000	18.94 ± 0.04ns	20.44 ± 0.04ns	20.08 ± 0.05ns

It can be seen that, when there is a transition from a 0 to 1 in the input data, the time interval between two recovered clock pulses decreases, as the number of consecutive zeros in the transmitted bit sequence increases. This is to be expected because, in the absence of a primary pulse, the recovered clock pulse advances Δ seconds later than the ideal time during each bit interval until a transition occurs. But, when there is a transition from 1 to 0 in the input data, the time interval between two clock pulses is greater (20.44 ± 0.04ns) than the interval between two clock pulses in the absence of transitions (20.08 ± 0.05ns). The interval between the clock pulses when a 1 to 0 transition occurs, depends on the transmitted bit sequence. Ideally, one would expect the time interval to be independent of the transmitted bit sequence. This unusual behaviour is also evident in Figures 6.7 (a) to (d) where the time interval between the recovered clock pulses (due to a primary and feedback pulse) varies from 0.095 ns to 0.16 ns.

The most probable reason for the difference in performance of the clock recovery circuit when triggered by a primary pulse and a feedback pulse is that the two pulse shapes are not exactly the same. To investigate this further, the two pulse shapes present at pin numbers 4 and 5 of IC3A (Fig.5.3) were measured, as shown in Figure 6.8(a) and (b). As is clearly evident from this figure, the primary pulse and the feedback pulse have different rise times and different slopes. It can be seen from Figure 6.8 that, the feedback pulse takes 0.8 ns longer time to reach the trigger level of 0.35V (50% of peak-to-peak amplitude). Since the feedback pulse has a smaller slope and larger rise time, it crosses the gate threshold at a time greater than $T+\Delta$ seconds. Thus, the recovered clock due to a feedback pulse occurs at a time greater than Δ seconds after the ideal time. Also the amplitude difference between the two pulses might be giving rise to amplitude-to-phase conversion.

The plausible reason for the larger rise time of the feedback pulse can be attributed to the distortion in the pulse shape which occurs as the pulse traverses through 4m. of RF coaxial cable (delay 1, Fig.5.3). The RF coaxial cable not only attenuates the pulse amplitude slightly, but also filters some high frequency components, thereby increasing the rise time of the pulse. Thus, even with this non-ideal behaviour the time difference is still very small and hence does not have much effect on the overall jitter performance.

In the next section we discuss the numerical results of the jitter measurement.

6.2 Bit-by-bit Jitter Measurements

The RMS value of the absolute jitter for the recovered clock depends on several parameters, i.e. laser diode, the fiber dispersion, the received power, the receiver transfer function and bandwidth, the received pulse shape, the APD gain, transmitted bit pattern, etc. In

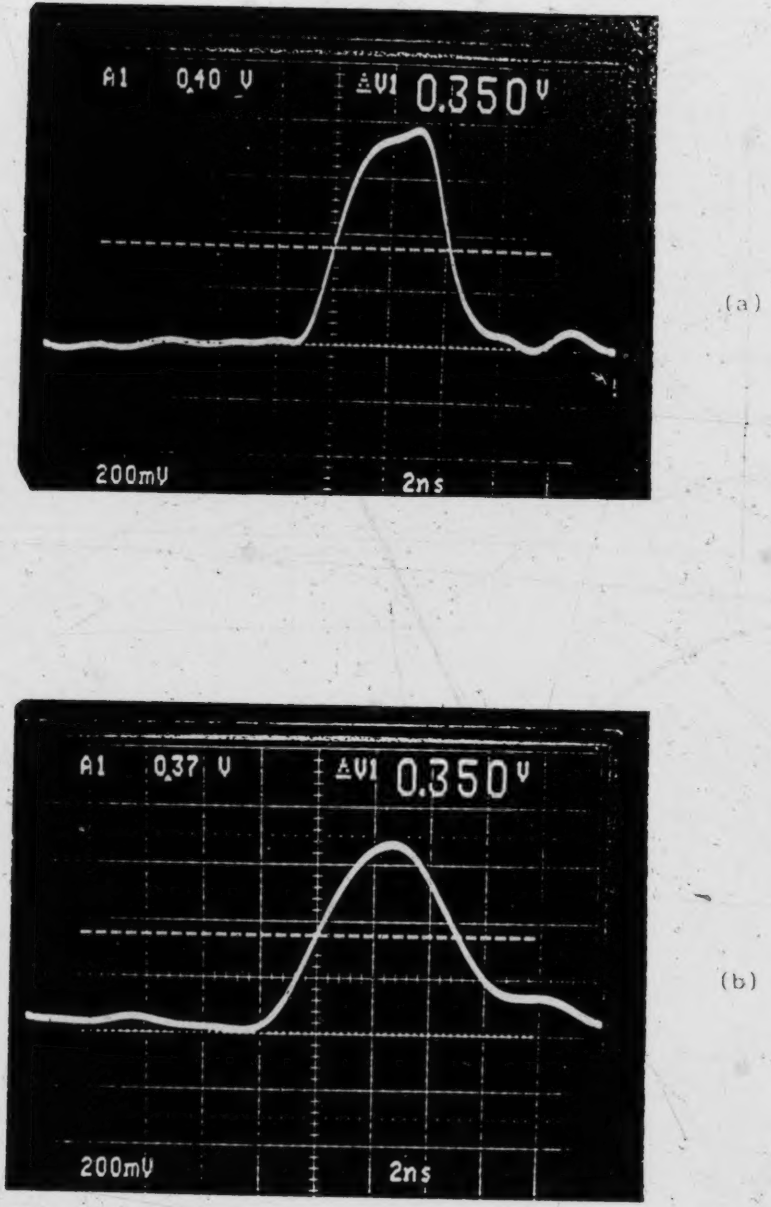


Fig.6.8 (a) Primary Pulse (Output of the Transition Detector)
(b) Feedback Pulse (at the end of Delay 1 of Fig.5.3)

this section, results are presented showing the variation of the RMS-jitter for different transmitted bit patterns, and for received power levels.

The jitter measurement technique described in Section 4.3 has been used to quantify jitter, given by the RMS value σ. The results presented here are for measurements done on the new clock recovery circuit. The recovered clock is at 50 MHz. Delay 1 was of duration 20.033 ns (Δ = 0.033 ns). The slope of the signal used to evaluate the timing jitter in Equation (4.9) was 3.68×10^{8} volts/second. The digitizing oscilloscope was set to a sampling speed of 100 MSamples/s on the real-time sampling mode. A transimpedance type of preamplifier was used, that had a frequency bandwidth of about 65 MHz; the low frequency 3 dB point was 20 KHz.

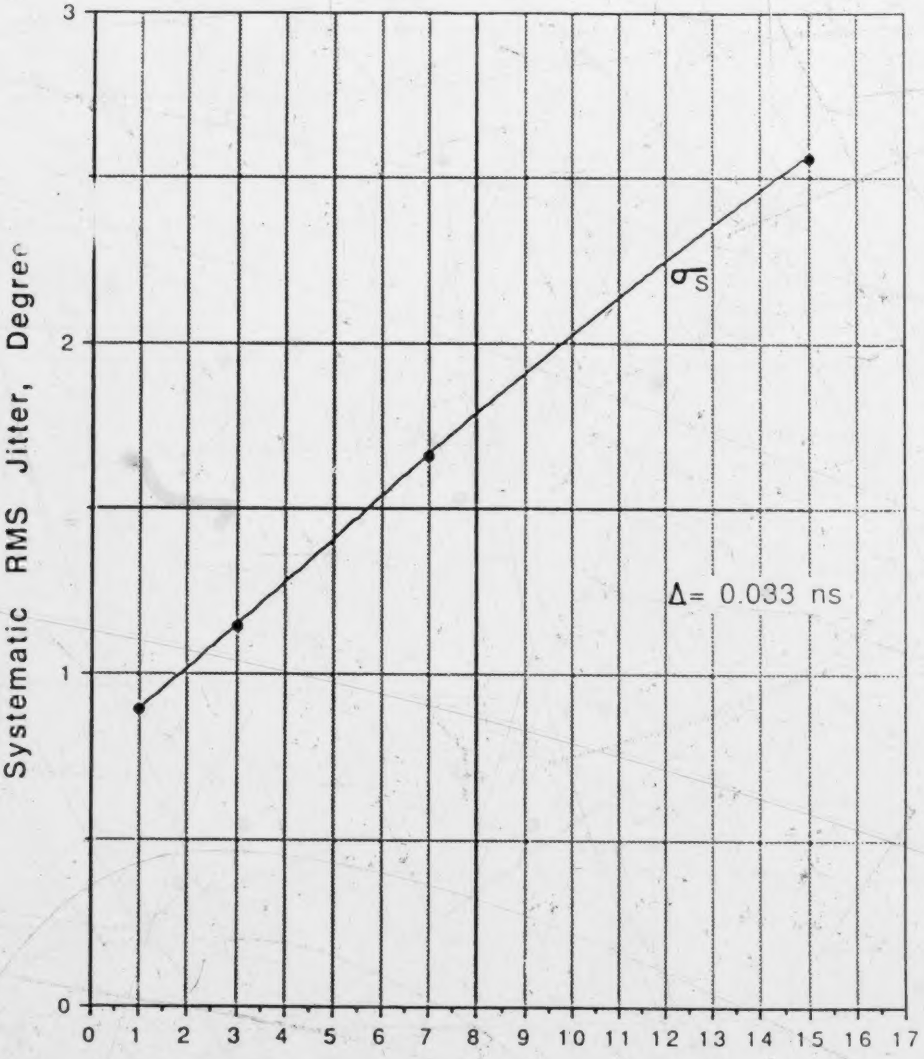
6.2.1 RMS Jitter versus Transmitted Data Pattern

Figure 6.9 illustrates the plot of *Systematic RMS Jitter* σ_s versus *transmitted data pattern*. The transmitted bit sequences are represented in terms of the number of consecutive zeros (Table 6.3).

Table 6.3

Transmitted Data Sequence (16-bit repetitive pattern)	No. of consecutive Zeros
1010101010101010	1
1000100010001000	3
1000000010000000	7
1000000000000000	15

The measurement results shown in Figure 6.9 were performed electrically using an RF coaxial cable as the communication link. The random jitter σ_R , which is caused by the noise present in the communication system now consists of only the thermal noise from the receiver amplifier electronics. We assume that this thermal noise is negligible and hence



No. of Consecutive Zeros ⟶

Fig. 6.9 RMS Systematic Jitter versus Transmitted Data Pattern

that the random jitter, σ_R, caused by this noise ~~is~~ also negligible. Since

$$\sigma_T = \sqrt{\sigma_S^2 + \sigma_R^2} \qquad \ldots(6.1)$$

where,

σ_T = Total RMS jitter
σ_S = Systematic RMS jitter
σ_R = Random RMS jitter

the measured total RMS jitter is approximately equal to the systematic jitter i.e. $\sigma_T \simeq \sigma_S$.

It can be noted from Figure 6.9 that the systematic RMS jitter, i.e., pattern-dependent jitter σ_S, increases with increasing Δ. This is to be expected because, as the number of continuous zeros or ones increases, the recovered clock pulse advances by Δ seconds (relative to the ideal time) during each bit interval, until a 0 to 1 transition occurs. In other words, as the number of transitions in the received bit pattern decreases, the RMS systematic jitter σ_S increases. The systematic jitter varies between 0.89° to 2.56° for 1 to 15 consecutive ones or zeros.

Measurements of jitter were also made with 5 km. of optical fiber in place. The amount of optical power falling upon the APD was -48 dBm. The average received optical power was measured using a Photodyne model 22XLA optical power meter, which has an accuracy of ± 0.1 dB. Figure 6.10 illustrates the relationship between the *Total RMS jitter* σ_T versus the *Transmitted data pattern*. Again, the transmitted bit sequences are represented in terms of the number of consecutive ones or

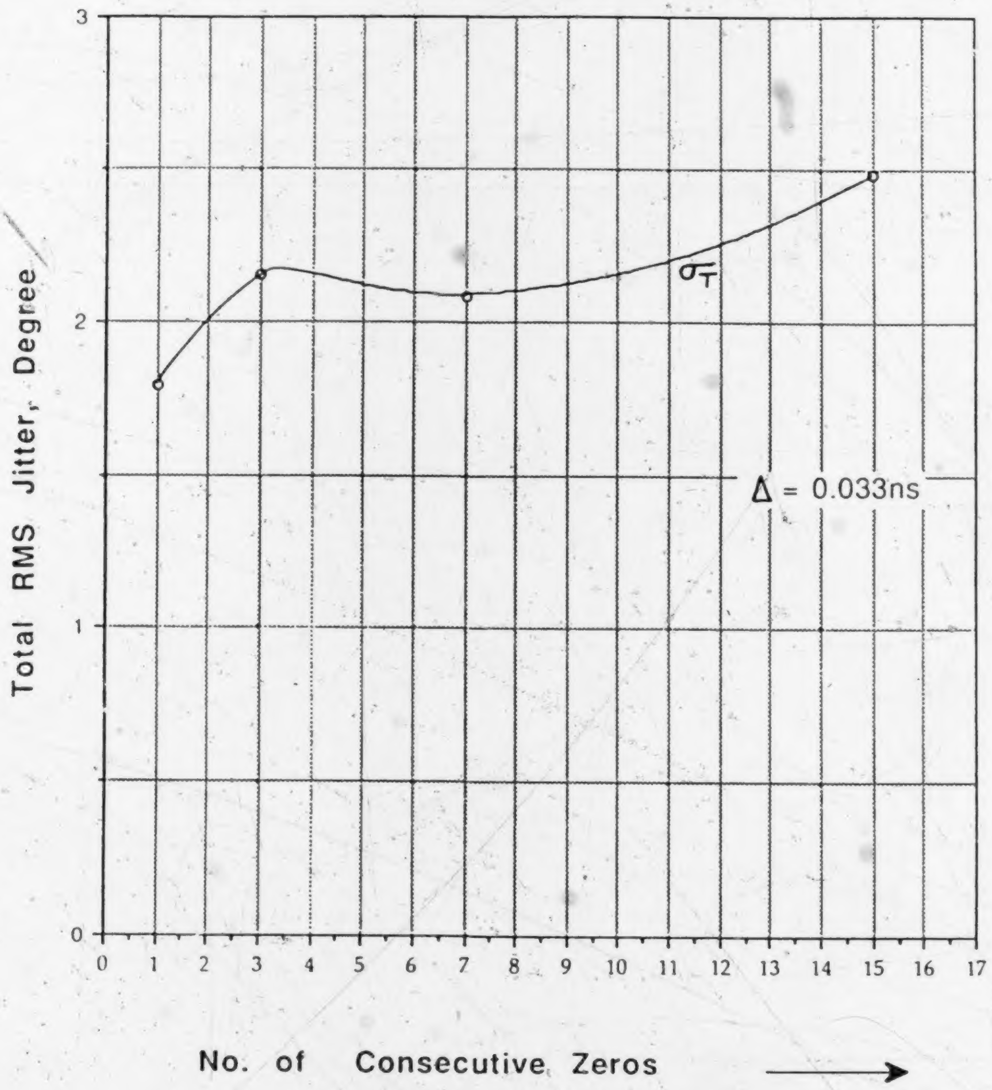


Fig.6.10 Total RMS Jitter versus
Transmitted Data Pattern
(Received Optical Power = -48dBm)

zeros (Table 6.3).

The measured total RMS jitter σ_T, now consists of the systematic RMS jitter; i.e., pattern-dependent jitter σ_S and the random RMS jitter σ_R, according to Equation (6.1). The random jitter is now caused mainly by the receiver shot noise due to the statistical nature of the photon-electron interaction.

We can observe from Figure 6.10 that the total RMS jitter σ_T also increases with an increase in Δ and it follows the same trend as in Figure 6.9. Comparing the two figures, we observe that σ_T is greater than σ_S for all the transmitted bit patterns except for 1000000000000000. This can be explained as follows:

When the measurements are performed electrically, only the pattern-dependent jitter or systematic jitter is present. For this case, therefore, the recovered clock pulses occur at the ideal time only when a 1 is present and advances Δ seconds later than the ideal time for the remaining 15 zeros, as the monostable multivibrator (MM) is triggered by the feedback pulses (see Fig.6.11). On the other hand, when the experiment is performed optically; i.e., when both systematic and random jitter are present, the recovered clock does not necessarily advance for 15 continuous bits giving the negative slopes in Fig.6.11. The MM is triggered not only by feedback pulses but also by pulses generated by noise. The pulses due to noise can occur at any time before the ideal time, so that, the overall spread of the occurrence of the clock pulses is less when both systematic and random jitter are present, than when only systematic jitter is present. See Fig.6.12. Hence, σ_T is less than σ_S for the bit sequence 1000000000000000. For a power level of -48 dBm, σ_T varies between 1.79° to 2.48° for 1 to 15

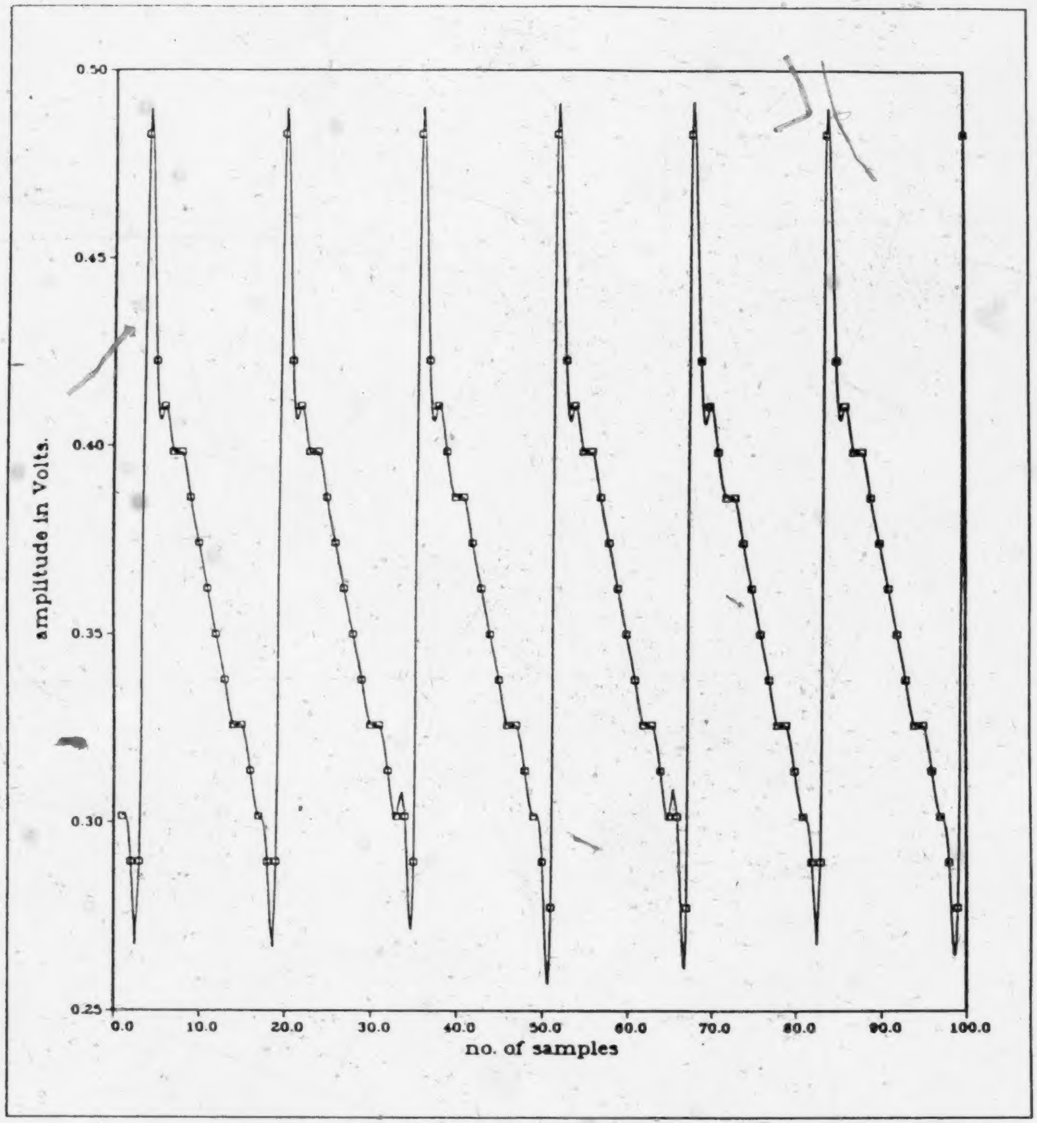


Fig. 6.11 Electrically Recovered Clock for an NRZ input of 1000000000000000, as it appears on the Screen of the Digitizing Oscilloscope (Δ = 0.033ns).

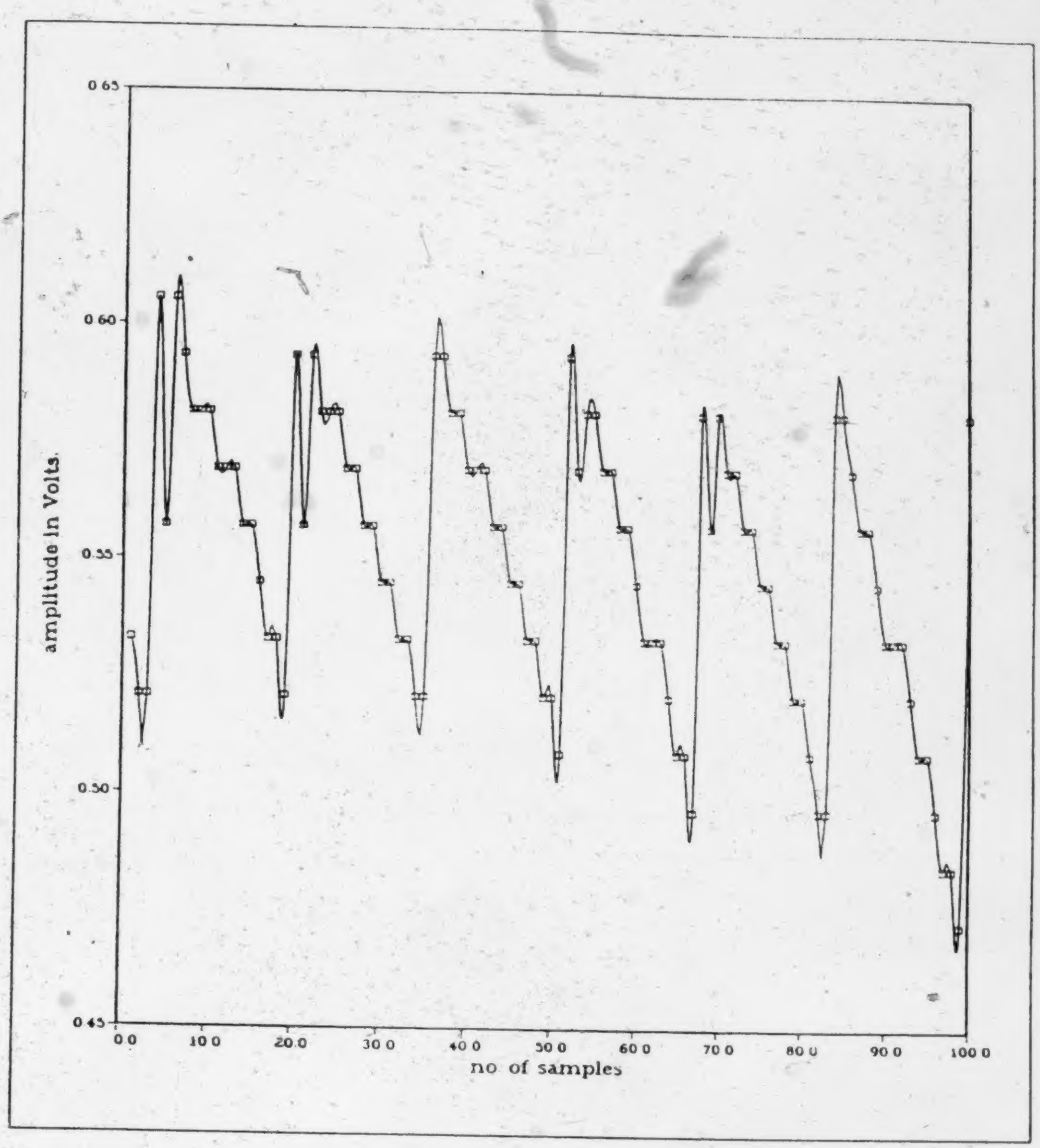


Fig. 6.12 Optically Recovered Clock for an NRZ input of 1000000000000000, as it appears on the Screen of the Digitizing Oscilloscope.
(Received Optical Power = -50dBm, Δ = 0.033ns)

consecutive ones or zeros.

6.2.2 Total RMS Jitter versus Received Optical Power

Figure 6.13 illustrates the relationship between the *Total RMS jitter* σ_T against *Received Optical Power Level*, for various 16-bit repetitive NRZ input data patterns. As an optical attenuator with proper matching connectors was not available, the amount of optical power falling upon the detector was varied by winding the optical fiber around a glass rod of diameter 2 cm. This gives rise to a controlled amount of microbending loss.

As can be observed from Fig.6.13, the total RMS jitter σ_T decreases as the received optical power level increases. This is to be expected, because the jitter variance is inversely proportional to the signal-to-noise ratio (SNR). As the power level increases, the random jitter σ_R due to noise decreases, whereas the systematic or pattern-dependent jitter does not change appreciably over the normal operating range. This can be seen by the flattening of the curves in Fig.6.13 for optical power levels above -48 dBm. The total RMS jitter σ_T settles down to a value of 1.5° to 2° in the normal operating range (above -48 dBm), which is essentially the systematic RMS jitter; i.e., $\sigma_T \simeq \sigma_S$. But at very low power levels, (less than -50 dBm) it is the random jitter which is dominant . Hence in the normal operating range, the systematic jitter is the primary cause of the recovered clock timing jitter.

From Fig.6.13 we also observe that, for a given received optical power level, the total RMS jitter σ_T increases as the number of transitions in the NRZ input data pattern decreases. This can be explained by the same argument as given in Section 6.2.1.

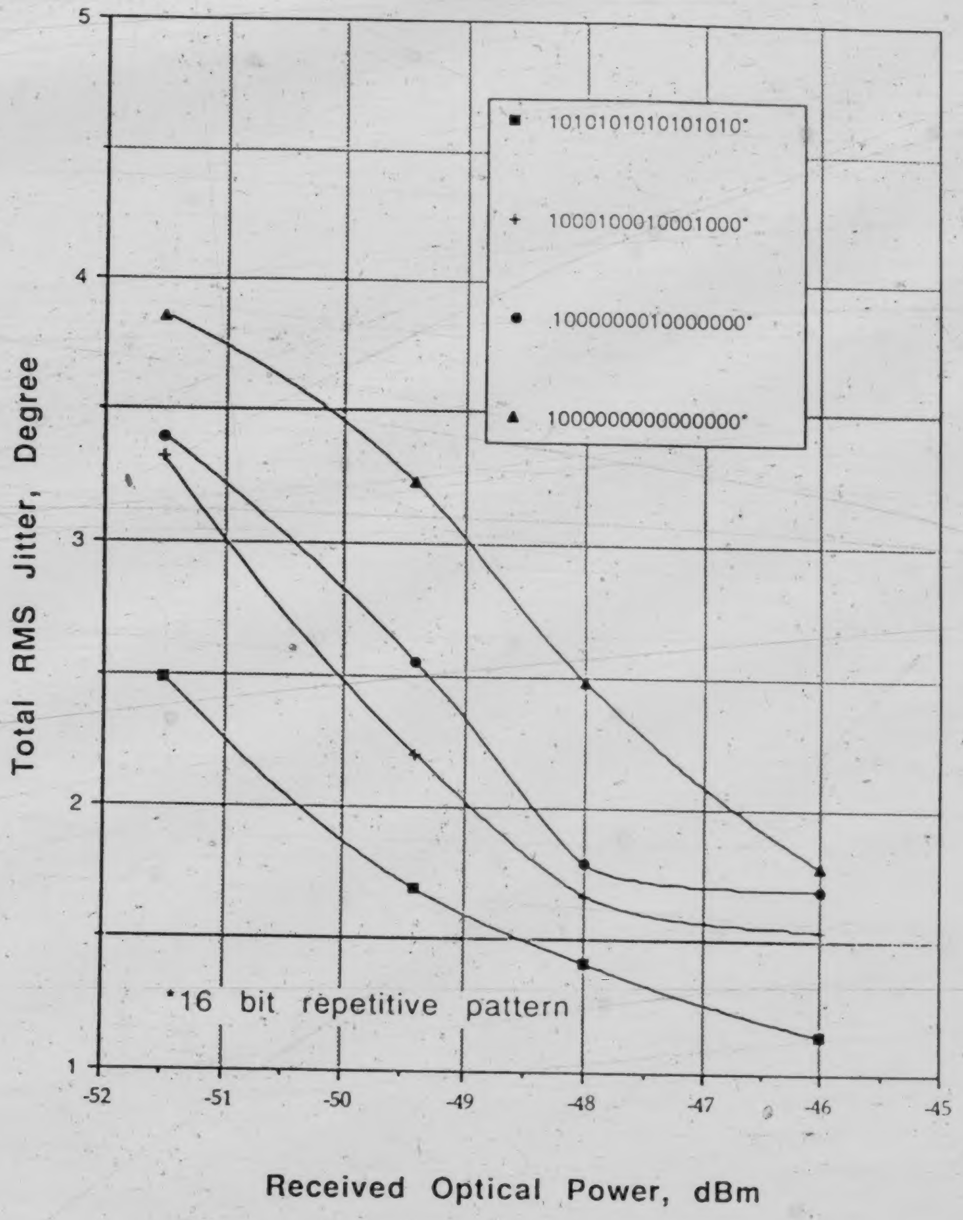


Fig.6.13 Measured Total RMS Jitter against Received Optical Power for a Fixed Pattern

Figure 6.14 illustrates the relationship between the *Total RMS Jitter* against *Received Optical Power Level* for NRZ pseudo-random bit sequences (PRBS) of length $2^{10}-1$ and $2^{23}-1$ respectively. Again the various optical power levels were achieved by winding the optical fiber around a glass rod.

It can be noted from Fig.6.14 that the total RMS jitter σ_T mainly consists of the systematic RMS jitter σ_S in the normal operating range of -49 dBm and above. It lies between 2° to 2.5° and is slightly larger than that for fixed word patterns. The systematic RMS jitter is higher for the PRBS of length $2^{23}-1$, as it has more pattern variations than the PRBS of length $2^{10}-1$.

At low power levels of -50 dBm and below, the random jitter due to noise, σ_R, is dominant. It lies between 3° to 4°. This large value is because, as the received optical power level decreases, more and more primary pulses trigger the MM earlier than the ideal time, causing the jitter variance to increase. As the optical signal power increases, the random jitter decreases significantly.

The RMS jitter for the two PRBS at low power levels (-51 dBm) should be close to each other around 4°. The wide difference in our case shown in Fig.6.14 might be due to some experimental measurement error. Nevertheless, the results presented in this chapter are comparable with other measurement techniques made on different clock recovery circuits [35,46,92,93].

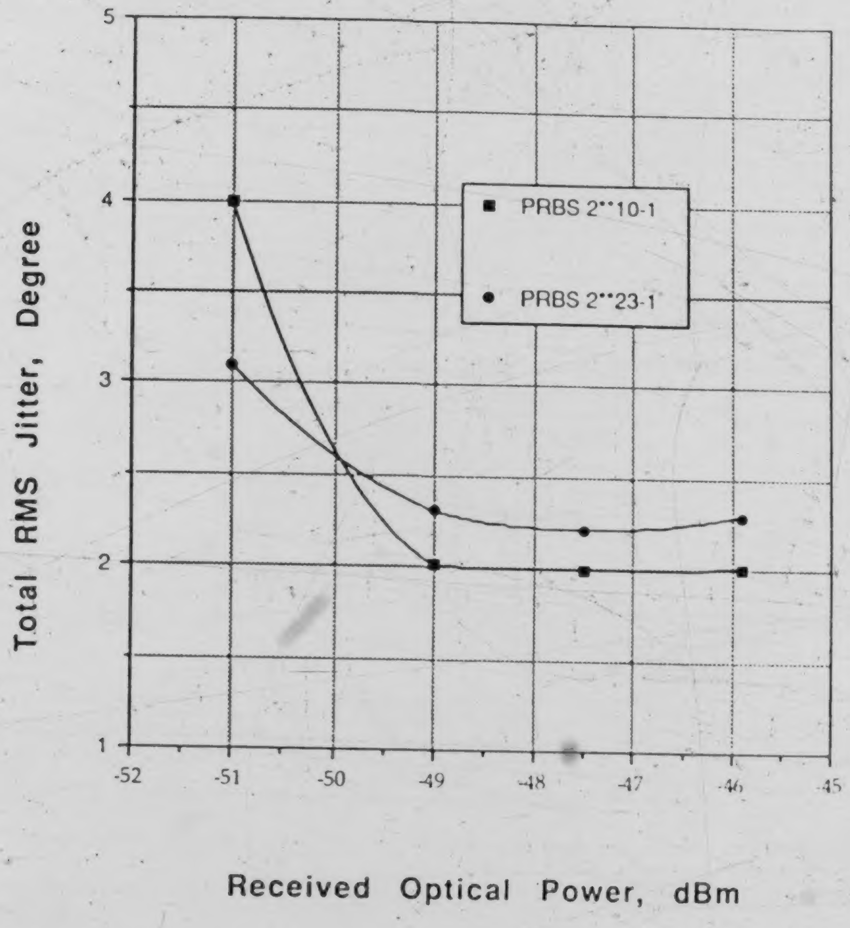


Fig.6.14 Measured Total RMS Jitter against Received Optical Power for Pseudo-Random Bit Sequence

CHAPTER 7

SUMMARY AND CONCLUSIONS

Telecommunication networks are increasingly employing digital technology to provide higher quality, less expensive, and more varied services to an increasing number of users. In a digital transmission system one important function of a communication receiver is to recover a sufficiently stable clock signal such that precise sampling instants can be generated in order to recover the original message signal. An unstable or jittering clock signal will impair the system BER performance. In other words, the BER deteriorates as the clock jitter increases. In order to quantify this important parameter and to assess the influence of jitter on the performance of an optical communication system, measurements of the amplitude distribution and RMS value of jitter are necessary [89,90].

Clock recovery at the receiver is normally a process of extracting a discrete component of the received signal spectrum at the pulse repetition frequency or one of its higher harmonics. As the spectral distribution of the received signal also contains the continuous spectrum, which tends to cause interference in the timing extraction process, the quality or stability of the recovered clock signal will depend on two major factors, namely: 1) the timing content of the received signal and 2) the characteristics of the timing extraction circuit at the receiver.

In this project, a bit-by-bit jitter measurement technique using a digitizing oscilloscope has been implemented to quantify the jitter generated in the new self-sustaining monostable multivibrator (MM) clock recovery circuit, originally developed by Witte and Moustakas

[70]. An NRZ type of line coding has been used for the input data.

A jitter measurement scheme has been implemented which provides a time and amplitude quantized histogram estimate for the probability density function of the timing jitter. It provides a statistical description, in that we can obtain the mean and the RMS value of the jitter phenomenon. The lowest jitter amplitude that can be measured is 1.7 ps. The peak-to-peak jitter that can be measured is limited by the linear rise time of the signal which in our case was 1.9 ns. The measurement scheme is dependent on the slope of the signal. The ultimate accuracy of the scheme is limited by the temporal and vertical resolution, the stability of the sampling, and the triggering and DC offset circuitry of the oscilloscope. Compared to earlier methods [75-83], this method has the advantage that an accurate estimate of the jitter variance can be obtained with no extra hardware circuitry. Also, the measurement scheme is independent of the data format. The measurement sensitivity could be improved by utilizing a digitizing oscilloscope having more bits of vertical resolution.

An experimental 50 Mb/s optical fiber communication system employing the NRZ code, and using the self-sustaining monostable clock recovery circuit was constructed and set up. Bit-by-bit jitter measurements were performed for various data patterns and for various received optical power levels.

During the course of the project it was observed that the primary pulses at the output of the transition detector in the original clock recovery circuit [70] did not occur at integral multiples of the bit period T. This was because the rising and falling edges of the input pulse had different gradients and hence they crossed the EX-OR gate threshold level at slightly different times. This was identifiable in this project only because the jitter measurements were made on a bit-by-bit basis, otherwise it could have gone unnoticed. This problem was overcome by replacing the EX-OR gate type of transition detector in [70] by a monostable multivibrator which triggers only on the rising edge. This has been referred to in this thesis as the "new version of the MM clock recovery circuit".

On obtaining the histogram estimate for the pdf of the timing jitter of the recovered clock, it was noted that the performance of the clock recovery circuit is different when it is triggered by a primary pulse or by a feedback pulse. Whenever there is a transition from a 1 to a 0 in the input data to the clock recovery circuit, the clock pulse due to the 0 bit does not occur Δ seconds after the ideal time (feedback delay $T1 = T + \Delta$), but occurs 0.095 ns to 0.16 ns later, depending on the transmitted bit sequence. This is due to the difference in the shapes of the primary pulse and the feedback pulse. The distortion in the feedback pulse shape is probably due to the filtering of high frequency components by the RF coaxial cable (feedback delay 1 of Fig.5.3), thereby increasing the rise time of the signal. A small improvement in the measured values might be possible, if some other means of providing feedback delay is incorporated.

The experimental results of measured RMS jitter versus transmitted data pattern confirm that the monostable clock recovery circuit inhibits the late arriving data pulses from triggering the monostable multivibrator. The clock jitter variance is proportional to the difference between the feedback delay and the bit interval, represented by Δ. The measured RMS jitter increases as the number of transitions in the data pattern decreases. At low received power levels the clock recovery circuit is triggered not only by the feedback pulses but also by false pulses caused by noise. This may cause the measured RMS jitter to decrease, especially if the bit sequence contains a long sequence of ones or zeros.

The measured RMS jitter against received optical power level demonstrates that the total RMS jitter decreases as the power falling on the detector increases. In the normal operating range, it is the systematic or pattern-dependent jitter that is dominant and it remains more or less constant throughout this region. Thus the jitter on the recovered clock in the normal operating range is due to the randomness of the received bit pattern. At low received power levels, the random jitter or bit transition jitter due to APD shot noise and additive circuit noise is dominant. The random jitter increases with decreasing optical power, but in the normal operating range, the pattern-dependent jitter is dominant.

Although this thesis has experimented with various jitter measurement techniques and investigated the jitter performance of the self-sustaining monostable clock recovery circuit, it was necessarily limited in its scope due to time constraints. To continue the work of this thesis, further research could be conducted in the following areas:

1. A widely used technique for the evaluation of a digital communication system is to obtain curves of bit error rate (BER) versus signal-to-noise ratio. It would be useful to obtain curves of BER against received optical power level with the jitter variance as a parameter to predict the performance of the experimental system.

2. It would be interesting to compare the experimental results obtained above with the theory. This would necessitate the evaluation of a theoretical expression for the probability of error, taking into account the time-dependent nature of the jitter pdf and the statistics of the line code.

3. The RMS value of jitter should be obtained for various amounts of feedback delay.

4. The jitter measurement range described in Section 4.3 is limited by the linear rise-time of the signal. One way to increase the measurement range is to integrate the recovered clock and then apply it to the digitizing oscilloscope. It would be worth trying this scheme experimentally.

5. The bit-by-bit jitter measurements should be repeated using the modified monostable clock recovery circuit, in order to determine its jitter performance.

6. To further characterize the monostable clock recovery circuit, it would be interesting to measure the power penalty versus jitter variance.

7. The time delays used in the clock recovery circuit were provided by a 50 ohm RF coaxial cable. This is not convenient for field use, because i) even a slight disturbance causes the output waveform to be distorted, ii) it is not convenient to change the length of the cable each time the amount of time delay needs to be changed, and iii) finally, the propagation delay of these cables varies with temperature. Hence, other methods of providing the delay should be investigated.

8. The accumulation of jitter produced by the self-sustaining

monostable clock recovery circuit over several repeaters must be studied before it could be considered for use in long-haul fiber optic systems.

9. The jitter produced by the self-sustaining monostable clock recovery circuit should be compared with other clock recovery circuits such as the dielectric resonator filter (DRF), surface acoustic wave filter (SAW), phase locked loop (PLL) and the LC filter. This could be done for various line codes, receiver bandwidths and noise characteristics.

10. Lastly, it would be useful to study the effect of Poisson distributed shot noise (such as is produced by an APD photodetector) on timing jitter, using a monostable clock recovery circuit.

It is sincerely hoped that the work done in this thesis may prove to be a useful contribution for future work on jitter measurement and analysis in clock recovery circuits for optical fiber communication systems.

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